Power Plane Spice Models for Frequency and Time Domains

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Abstract
A spice model for power plane simulation has been developed. It is based on the geometries and materials of the power planes and uses a unit cell composed of RLC elements, transmission line elements or the W-element. Important frequency and time domain properties are demonstrated through simulation and model to hardware correlation is established in both domains.

Introduction

Power planes are used to deliver power to both logic core and I/O circuits on modern computer systems. With each computer generation, the amount of power required is ever increasing. As silicon technology advances, scaling has required that the power supply voltage be reduced. Since the current delivery requirements on the power planes have gone up and the tolerance for noise has gone down, the power planes are required to be lower impedance from DC to high frequency, possibly several GHz (1).

This paper will examine the characteristics of power planes in delivering low impedance power at high frequency. A method of modeling the power planes is given. The advantages of several base unit cells are discussed. The model is used to examine important power plane properties in the frequency and time domains. The power plane model is correlated to hardware measurements.

Model Parameters

Power Planes are easily modeled as an array of circuit elements (2). The circuit elements have been simulated in the Avanti Star HSpice simulator (3). The parameters of these elements are based on some simple calculations that relate directly to the materials and geometries used to construct the power planes (4). Power planes are formed by two parallel plates of conducting material separated by a dielectric. As a first approximation, this is a parallel plate capacitor that has Capacitance per area:

$$C_a = \frac{\varepsilon}{thickness} \qquad (farads/unit\_area)$$

where $\varepsilon = \varepsilon_0 \varepsilon_R$ is the electrical permittivity. The velocity of a plane wave traveling between the parallel plates of this capacitor is:

$$velocity = \frac{c_{light}}{\sqrt{\varepsilon_R}} = \frac{1}{\sqrt{L_a \cdot C_a}}$$

where ε_R is the relative permittivity of the dielectric and c_{light} is the velocity of light in free space. The simple relationship between inductance per square (L_a), capacitance and velocity enables the calculation of inductance:

$$L_a = \frac{1}{c_a \cdot velocity^2} \qquad (henries/square)$$

From inductance and capacitance, the impedance and delay of transmission lines are easily calculated:

$$Z_0 = \sqrt{L_a / C_a} \qquad t_{delay} = \sqrt{L_a \cdot C_a}$$

Of the four parameters: inductance, capacitance, impedance and velocity; only two are independent. Any two may be used to calculate the other two and delay is the reciprocal of velocity. The above calculations are sufficient to derive either lumped element or transmission line parameters that describe the behavior of lossless power planes.

Loss on power planes is attributed to three phenomenon: DC copper resistance, skin effect resistance for the conductor and dielectric loss for the insulator. The DC resistance is independent of frequency. Skin effect causes current to travel in the conductor at a depth that is proportional to sqrt(frequecy). After the onset of skin effect, an ever diminishing surface depth carries current as frequency increases. The resistance of the power plane conductor is:

$$R = \frac{length}{width} \frac{1}{\sigma \cdot \min(thickness, \delta)}$$

$where:$

$$\delta = \frac{1}{\sqrt{frequency \cdot \mu\pi\sigma}}$$

$$\sigma = conductivty\ of\ conductor$$

$$\mu = permiability\ of\ conductor$$

Dielectric loss is due to the conductivity of the dielectric which is proportional to frequency and capacitance:

$$G = \omega \cdot C \cdot \tan\Delta$$

where $\tan\Delta$ is the loss tangent of the material, assumed to be constant with frequency.

Model Topology

The physical features of the power planes and the high level circuit model composed of unit cells are given in figure 1a. The parameters above are used to build three different unit cells for the power plane model. The circuit topology for the base cells are given in figure 1b, c & d, and involve RLC lumped elements, the spice T-element and the

StarHspice W-element. Transmission line elements in both the x and y direction tend to "double count" the capacitance of the power plane. To account for this, the impedance is increased and the time of flight is decreased by a factor of sqrt(2). This causes the total capacitance of the power planes and the time delay across the power planes to simulate correctly with the given topology.

The topology of figure 1 involves an 8x8 array of unit cells but other grid granularity is possible. For spice modeling, it is convenient to choose a grid granularity and calculate model parameters from plane materials and geometries. The topology remains constant and the parameters are calculated within the spice execution. The alternative is to calculate "per unit area" model parameters and change the topology (add or subtract unit cells) according to the size of the planes. This usually requires some scripting outside of the spice executable to build the model topology.

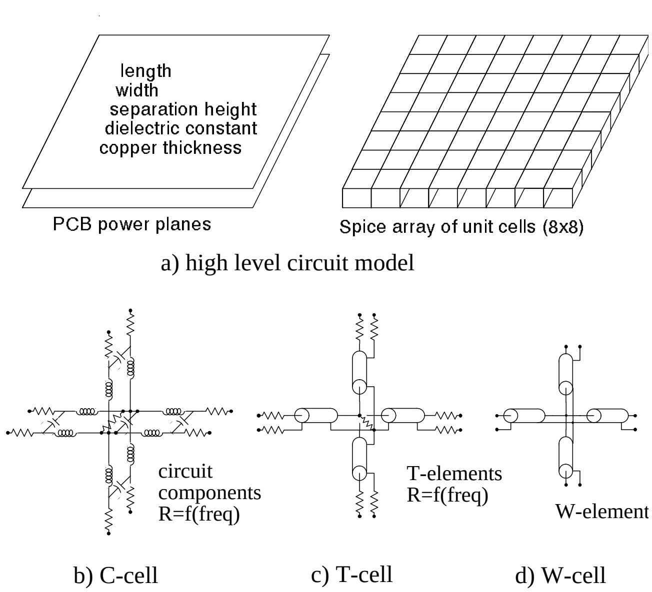

Figure 1: Circuit Elements for power plane spice model.

The granularity of the model has definite implications on run time and accuracy. Transmission lines exhibit resonant phenomenon when they are not properly terminated in their characteristic impedance. Of particular importance are the half and quarter wavelength frequencies where standing waves develop or impedances are inverted. The topology of the plane models gives transmission lines that are inherently miss-terminated at each node because one transmission line is feeding the parallel combination of 3 similar transmission lines. It has been empirically determined that the maximum length of a transmission line segment should be no more than 1/5 of a rise time for a transient simulation. This enables the near end of each transmission line to influence the far end twice during the rise time. Using the relationship of frequency content being 0.35/tRise, the transmission line should be no longer than 1/15 of a wavelength long at the maximum frequency of interest.

The model is used to simulate power planes that are 6 inches square and separated by an $\varepsilon_R = 4$ dielectric. The results are shown in figure 2. A total of one amp is injected into one side of the planes, so the voltage magnitude measured at any point on the planes is equivalent to impedance or transimpedance for the stimulated plane edge. The transmission line segments between nodes were 3/4 inch or 125 pSec long and the rise time in the transient run is 625 pSec, giving smooth edges. The frequency where lambda is 15 x 3/4 = 11.25 inches is 533 MHz. This simulation appears to be good up to 3 GHz, but that is because the plane edge is stimulated so that the wave front propagates down the length of the planes. There is no loading along the width dimension. For simulations involving a point source (i.e. spreading inductance), frequency domain results are valid up to just 533 MHz.

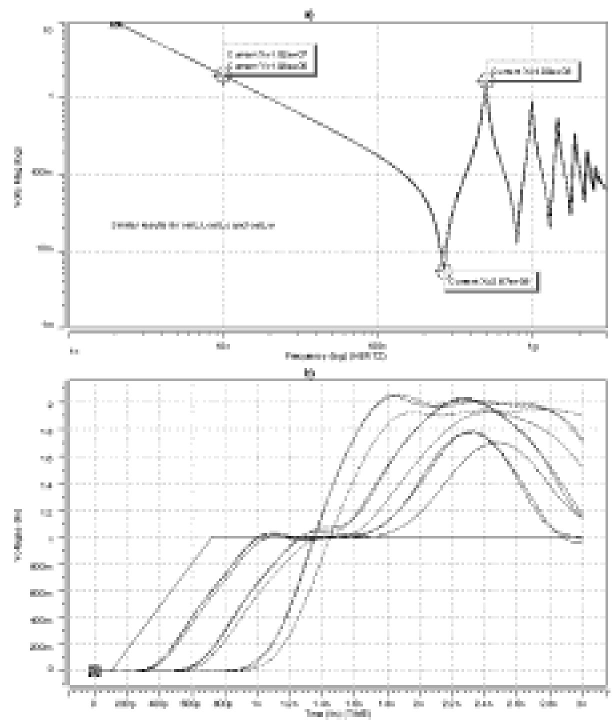

Figure 2: model simulation a) frequency domain b) time domain.

Model Performance

The CPU run times for frequency and time domain simulations using the 3 base cells are compared:

cell	ac time	tr time	total	units
C	18	3	21	seconds
T	21	5	26	seconds
W	84	29	113	seconds

For all three base cells, the frequency domain results have the correct frequency dependent loss because frequency dependent resistors or the W-element account for the loss.

The three overlapping curves are shown in 2a. Only the W-element gives correct frequency dependent results in the time domain. There is a substantial CPU time penalty for this accuracy.

Power Plane Properties

At low frequencies, the power planes behave like a parallel plate capacitance. The 6 inch square planes simulated above have 4 mils of $\varepsilon_R = 4$ material separating them. The capacitance is calculated:

$$Capacitance = C_a \cdot area = \frac{\varepsilon_R \varepsilon_0}{thickness} \cdot length \cdot width = 8.1nF$$

The impedance of 8.1 nF at 10 MHz is:

$$Z = \frac{1}{j\omega C} = 1.96 \qquad ohms$$

Figure 2a shows that the self impedance of the planes measured at the stimulated edge. The impedance at 10.02 MHz is 1.98 Ohms, very close to what is expected. 000

Figure 2b shows how the edge propagates along the plane. When the pulse hits the open circuit edge of the planes, it doubles and reflects back. The delay for the edge is the same as that of a signal transmission line, about 170 pSec per inch.

The time delay for the RLC components and the spice T-element are similar but the delay for the W-element is about 8.6% longer. This apparently is because the frequency dependent loss reduces the amplitude of the signal for a small amount of time, giving the appearance of additional delay for the edge.

Frequency Domain

The time delay across the 6 inch planes is 1 nSec and one wavelength will stand in the resonant cavity at 1 GHz. One half wavelength will stand in the cavity at 500 MHz and the quarter wave length frequency is 250 MHz. Note that in figure 2a, there is a low impedance dip at 250 MHz. That is because the open circuit at the far end of the 6 inch planes appears to be to be a short circuit at the quarter wavelength frequency. There is a resonant peak at 500 MHz. That is because a half wavelength stands in the cavity at that frequency. There is high voltage at each end of the planes and high current in the center of the planes at the half wavelength frequency.

Similar effects are demonstrated for all of the quarter wavelength frequencies (3/4, 5/4, 7/4, 9/4, ...) and all of the half wavelength frequencies (1, 3/2, 2, 5/2, ...). These are responsible for the high impedance peaks and the low impedance dips. Note that as the frequency increases, the magnitude of the peaks and dips diminishes. That is because frequency dependent loss (skin and dielectric) increases with frequency and the Q of the resonator drops with increasing loss. This model is used to investigate the damping properties of plane materials & geometries and is documented in (5).

Figure 3a shows the same power planes stimulated with 1 AC amp injected between the planes in a position that is on the left hand edge. The several traces are the voltage measured at several of the 64 nodes on the power planes. The heavy black trace is the impedance measured at the injection point and the other nodes are the transimpedance response to the stimulation. Notice that many of the traces peak at the same frequency because of the cavity dimensions. The dips are all at different frequencies because they are associated with 1/4 wavelength from the measurement point to an open edge of the planes. At frequencies well below that of the first resonant dip, all points on the board are at the same voltage. Components placed anywhere on the board will see the same voltage across the power supply. But at higher frequencies above the first resonant dip, position on the board is extremely important.

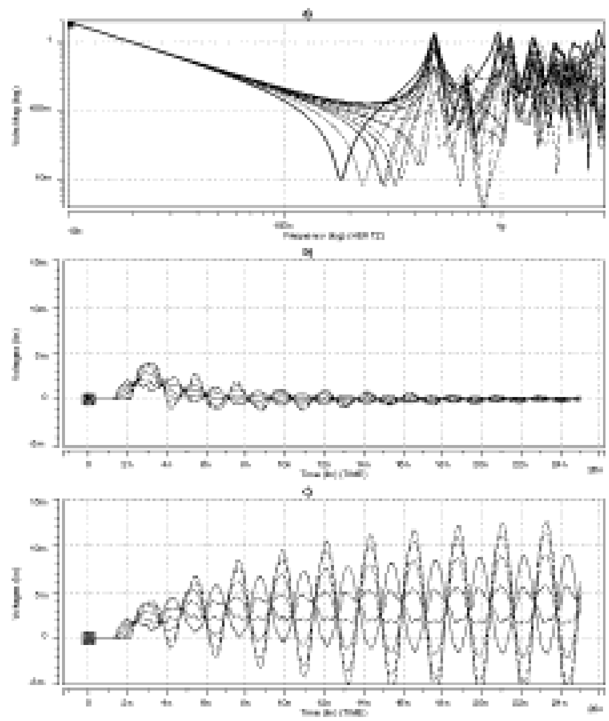

Figure 3: simulation from point source: a)frequency domain, b) time domain single pulse, c) 500 MHz pulses.

Time Domain

Figure 3b shows the same power planes stimulated by a time domain pulse. A 1 volt source has been connected to the planes through a 50 ohm resistor. The several traces are at adjacent points along the plane in one direction. Figure 3c shows the same stimulation but with a 500 MHz pulse train which matches the cavity resonant frequency as determined by the dimensions of the plane and dielectric constant. The first edge does not create much disturbance. But as edges continue to reinforce each other at the resonant frequency, each pulse puts a little more energy into the cavity.

Cavity resonances build up until the losses due to copper resistance, skin effect and dielectric balance the energy that is delivered by the source.

Problems will arise on product boards that happen to stimulate a resonant peak with a clock or clock harmonic frequency unless there is sufficient damping at that frequency to absorb the energy. The first edge flows out from the source in a radial fashion. But as time goes on and each edge reflects off the sides of the planes. The wave fronts are no longer radial but become plane waves perpendicular to the square edges of the planes.

Model to Hardware Correlation

Model to hardware correlation is obtained in the frequency domain by using a vector network analyzer (VNA) and making S21 measurements (7). A bare printed circuit board with no components attached is used for the measurements. Port 1 and Port 2 are attached to decoupling capacitor pads on opposite sides of the board by soldering down 50 ohm coax with short connections. Calibration was done by soldering the 50 ohm coaxes together with no DUT. The "through" calibration was set to 0 dB. The parallel combination of the two coaxes is 25 Ohms, which becomes the reference impedance. The VNA gives readings in dB, which are converted to impedance by the equation:

$$dB = 20Log_{10}\left(\frac{z\ plane}{25}\right)$$

Figure 4a shows the simulated and measured impedance of a 20.5x10 inch pair of power planes with 2 mils separation. The same power planes were stimulated with a pulse data generator at the same positions. The pulse generator drove 0 volts for a long time and then a square wave at 140 Mhz, one of the resonant peaks from the frequency domain measurements. Figure 4b shows the simulated and measured results.

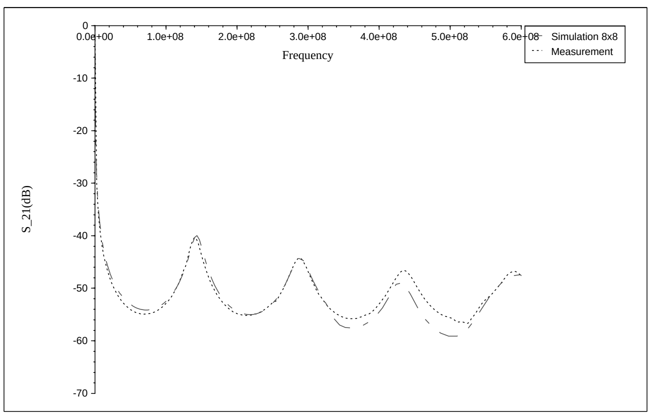

Figure 4a: Simulated and measured power plane impedance in the frequency domain.

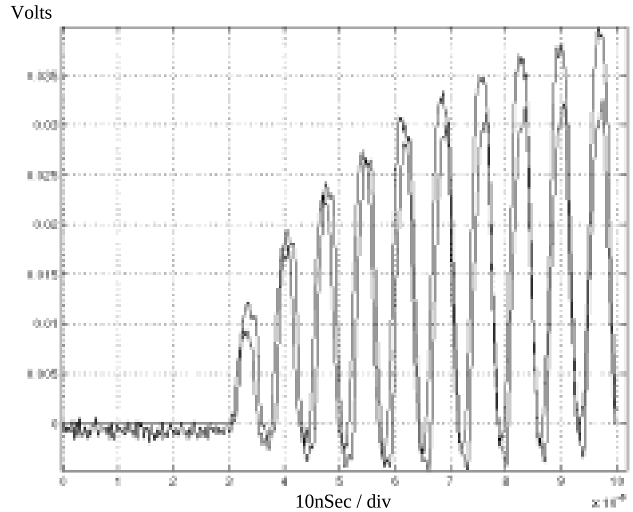

Figure 4b: Simulated and measured time domain response

Conclusions

Low power plane impedance at high frequency is important for the power distribution systems of modern computers. A simple method of simulating the power planes in spice has been presented. Unit cells based on lumped elements, ideal transmission lines and lossy transmission lines have been demonstrated, each with their own advantages and disadvantages. Model to hardware correlation has been shown in the frequency and time domains.

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