LARRY SMITH

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PRINCIPAL ENGINEER – TECHNICAL LEAD

Optimize Performance and Cost Savings Simultaneously to Deliver Innovative Technical Solutions

Power Integrity expert with patents on simulation and measurement techniques to manage power integrity and PDN design. Adept in quantifying the contributions of the board, package and die, providing high-quality power to silicon circuits. Guide cost and performance discussions in cross-functional teams, influencing decision making on business and technical planning. Recently published book: “Principles of Power Integrity for PDN Design.”

- Team Leadership
- Methodology Development
- Lab Characterization
- Project Management
- ADS
- SPICE
- Excel
- VNA
- Oscilloscope
- Patents
- Cost Controls
- Compliance

PROFESSIONAL EXPERIENCE

QUALCOMM INC., San Diego, CA

Principal Engineer - Power Integrity Technologist (2011 to 2018)
Quantified maximum amount of transient current a PDN can deliver with acceptable voltage droop. Defined Intellectual Property (IP), package and board facing PDN specifications. Quantified cost and performance trade-offs. Developed Lab measurements to correlate with simulations.

- Optimized costs and performance by developing PDN Resonance Calculator (PRC) tool and simulation techniques to define PDN capabilities for cross-functional team.
- Defined the amount of transient current a PDN can deliver with acceptable voltage droop based on board, package and IP facing specs, providing a basis for future PDN design and architecture.
- Developed convolution technique to check compliance of PTPX current vectors with IP facing specifications.
- Quantified several loss and damping mechanisms that control height of PDN impedance peak, enabling cost and performance optimization.
- Measured and modeled discreet MLCC capacitors in a way that stabilized transient simulations based on S parameters thus resulting in reliable PDN simulations.
- Developed PDN sense line measurement techniques for enabling complete PDN characterization and correlation.
- Worked within cross-functional teams (Packaging, PMIC, Customer Engineering, and Architecture) in analyzing and translating requirements into optimal solutions to ensure schedules and milestones were met.

ALTERA, San Jose, CA

Architect (2005 to 2011)
Managed all aspects of signal and power integrity and cross-functional optimization of FPGA products for best cost and performance.

- Achieved product cost savings by reducing package layers and solving major signal integrity problem.
- Achieved high performing and cost-effective FPGA solutions for signal and power integrity by collaborating with circuit designers, packaging, characterization, board design, customer engineering and marketing.
- Established methodology for developing adequate power distribution networks to deliver FPGA power, establishing the PDN design methodology.
- Saved $7M annually by utilizing measurement techniques to propose and validate design changes, reducing package layer count from 14 to 10.
- Developed PDN tool to optimize board and decoupling capacitor configurations which is still used today and rated 1 of the top 10 free SI/PI tools available.
- Established a number of return paths necessary to carry IO return current and guided cross-functional team to consensus, bringing company out of a major customer signal integrity problem.
- Established impulse, step and resonance responses as the best way to characterize PDNs which became an industry standard technique.

SUN MICROSYSTEMS, Menlo Park, CA

Principal Engineer (1996 to 2005)
Provided technical insight on signal and power integrity in central engineering group. Established original concepts and simulation techniques for power integrity. Defined target impedance and spreading inductance in IEEE Journal papers.

- Designed and patented 6 techniques used in Sun PDN designs and sold to Cadence as the first power integrity tool, establishing the phrase 'power integrity' industry-wide.
- Developed frequency domain target impedance methodology for quantifying the number and types of decoupling capacitors for an optimum PDN.
- Delivered one of the first power plane simulators for resonances and decoupling capacitor placement.
- Established relationship between power plane bounce and signal return currents that influenced all Sun product designs.

ADDITIONAL EXPERIENCE

IBM, Essex Jct, VT; San Jose, CA

Advisory Engineer
Advised on circuit and package design, silicon characterization, on-die power distribution and reliability. Developed initial power distribution system management techniques that are now used industry-wide. Established power supply target impedance concept. Defined, developed and articulated frequency domain techniques for managing power distribution in publication before PDN and power integrity were recognized words and phrases in the industry.

EDUCATION

Master of Science in Material Science (MSMS)
UNIVERSITY OF VERMONT, Burlington, VT

Bachelor of Science in Electrical Engineering (BSEE)
ROSE HULMAN INSTITUTE OF TECHNOLOGY, Terre Haute, IN

AFFILIATIONS & PATENTS

Senior member of IEEE
More than 12 patents

SAMPLE OF PUBLICATIONS

Available for download at pdnpowerintegrity.com

Larry D Smith, Eric Bogatin, *Principles of Power Integrity for PDN Design*. Prentice Hall, 2017

“A Convolution Technique for Verifying Acceptable PTPX Current Waveforms for PDN Voltage Droops” DesignCon 2018, Larry D Smith, Yi Cao

“Impedance and Transient Current Fundamentals” DesignCon Tutorials 2015 and 2018, Larry D Smith

“Novel Parallel Resonance Peak Measurement and Lossy Transmission Line Modeling of 2-T and 3-T MLCC capacitors for PDN Application” ECTC 2017, Varin Sriboonlu, Larry Smith

“PDN Resonance Calculator for Chip, Package and Board” DesignCon 2012, Larry D Smith, Mayra Sarmiento, Yuri Tretiakov, Shishuang Sun, Zhe Li, Sunitha Chandra

“On-Die Capacitance Measurements in the Frequency and Time Domains” DesignCon 2011, Larry D Smith, Shishuang Sun, Mayra Sarmiento, Zhe Li, Karthik Chandrasekar

“On-Chip PDN Noise Characterization and Modeling” DesignCon 2010, Shishuang Sun, Larry D Smith, Peter Boyle

“System Power Distribution Network Theory and Performance with Various Noise Current Stimuli Including Impacts on Chip Level Timing” IEEE Custom Integrated Circuits Conference, September 2009, Larry Smith, Shishuang Sun, Peter Boyle, Bozidar Krsnik

“FPGA Design for Signal and Power Integrity” DesignCon 2007, Larry Smith, Hong Shi

“Frequency Domain Target Impedance Method for Bypass Capacitor Selection for Power Distribution Systems” DesignCon 2006, Larry D Smith

“MLC Capacitor Parameters for Accurate Simulation Model” DesignCon 2005, Larry D Smith

“Power Distribution System for JEDEC DDR2 Memory DIMM” IEEE Electrical Performance of Electronic Packages 2003 (EPEP 2003), Princeton, NJ, .pp 121-124 Oct 2003 by Larry D. Smith and Jeffrey Lee

“A Transmission-Line Model for Ceramic Capacitors for CAD Tools Based on Measured Parameters” Conference Record, Electrical Components Technology Conference (ECTC) May 2002, San Diego, CA, by Larry D. Smith, David Hockanson, Krina Kothari

“Model to Hardware Correlation for Power Distribution Induced I/O Noise in a Functioning Computer System” ECTC 2002 at San Diego, CA, by Sungjun Chun (GaTech), Larry Smith, Ray Anderson, and Madhavan Swaminathan

“Distributed SPICE Circuit Model for Ceramic Capacitors” IEEE ECTC Conference, Lake Buena Vista, Florida May 29-June 1, 2001 by Larry Smith and David Hockanson

“Chip-Package Resonance in Core Power Supply Structures for a High-Power Microprocessor” Proceedings of IPACK'01, the Pacific Rim/ASME International Electronics Packaging Technical Conference and Exhibition, July 8-13, 2001, Larry Smith, Raymond Anderson, Tanmoy Roy

“Power Plane SPICE Models and Simulated Performance for Materials and Geometries” IEEE Transactions on Advanced Packaging, Vol.24, No.3, August 2001 pp277-287. Larry Smith, Raymond Anderson and Tanmoy Roy

“Power Distribution System Design Methodology and Capacitor selection for Modern CMOS Technology” IEEE Transaction on Advanced Packaging, August, 1999 pp284-291. Larry Smith, Raymond Anderson, Doug Forehand, Tom Pelc, and Tanmoy Roy

“Simultaneous Switch Noise and Power Plane Bounce for CMOS Technology” IEEE Electrical Performance of Electrical Packaging (EPEP) Conference, San Diego, CA Oct 17-25, 1999 by Larry Smith

“A CMOS-Based Analog Standard Cell Product Family” IEEE Journal of Solid State Circuits, Vol.24, No.2, April 1989, pp370-379. Larry D. Smith, H.R. Farmer, M. Kunesh, M.A. Massetti, D. Willmott, R. Hedman, R. Richetta, T.J. Schmerbeck