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Power Distribution System for JEDEC DDR2 Memory DIMM

Larry D Smith, Jeffery Lee
Sun Microsystems, Inc. MS MPK15-103
15 Network Circle, Menlo Park, CA 94303-4900
Phone: 650-786-3303, FAX: 650-786-6457
larry.smith@sun.com jeffrey.lee@sun.com

Abstract - The Power Distribution System (PDS) for a JEDEC DDR2 Dual Inline Memory Module (DIMM) has been designed. The process involved establishing a target impedance in the frequency domain, determining the inductance of the connector and capacitor mounts and selecting a matrix of discrete ceramic capacitors from a menu of previously characterized devices to meet the target impedance. After hardware was available, S21 measurements were made with a 2 port VNA to establish model to hardware correlation.

Introduction – Advanced Memory DIMMs may draw 10 watts of power or more and it is necessary to carefully design the PDS to supply the high currents at low voltage. Low frequency power comes from a mother board through a DIMM connector. The connector inductance limits the maximum power transfer frequency to about 1 MHz. Capacitors mounted on the DIMM power planes supply current from 1 MHz up to the frequency where the inductance of the memory-chip package limits the current, about 100 MHz. Capacitors are chosen for the DIMM PDS so that the impedance seen by the chips is less than or equal to a target impedance in the 1 to 100 MHz range. Above 100 MHz, power must be supplied by on-chip decoupling capacitance.

Target Impedance – First, the target impedance is established for the DIMM [1]. The target impedance is calculated from the allowable voltage tolerance for the chips and the maximum expected transient current using the formula:

$$Z_{target} = \frac{voltage\ tolerance}{transient\ current} = \frac{Vdd \times n\,\%}{I_{max} - I_{min}} = \frac{1.8V \times 5\,\%}{(Idd7 - Idd2) \times 18\ chips} = \frac{1.8 \times 0.05}{(400\ mA) \times 18} = 12.5\ mOhms$$

The maximum current drawn by each chip is Idd7, which may happen several times in a row and last for 100's of nSec. The minimum current is associated with the idle current, Idd2. All of the 18 memory chips on the DIMM can be in the Idd7 or Idd2 mode at the same time. A 12.5 mOhm target impedance is therefore established for the DDR2 DIMM. From the memory circuits standpoint, the target impedance should be met from DC up to the maximum frequency at which the circuits draw current. It is possible for customer code to cause the chip to demand current at virtually any sub-harmonic of the clock (access cycle) so it is best if the PDS has a flat impedance profile with frequency. If the Impedance of the DIMM PDS is higher than the target impedance between 1 and 100 MHz, the power supply voltage may exceed the 5% voltage margin. Cost is optimized when components are selected so that the PDS meets the target impedance but does not fall too far below it.

Inductance – Series inductance in the PDS limits the amount of current that can flow at a given frequency. Inductance comes from the magnetic field which surrounds all conductors that carry PDS current including the DIMM connector, power planes, chip-package conductors and mounting structures for decoupling capacitors. The maximum effective frequency for a conductor may be found by comparing it's reactance ($j\omega L$) to the target impedance.

For example, the loop inductance for the power pins in the DIMM connector limits the frequency at which power may be drawn from the mother board. The inductance of the connector is measured using a parallel resonance technique. This is done by shorting Vdd to Gnd and resonating the shorted loop inductance with the printed circuit board power plane capacitance. All pins on the mother board side of the unattached DIMM connector are shorted with copper tape and solder. An unstuffed (bare fab) DIMM PCB is inserted into the shorted connector forming an inductive path between the Vdd and Gnd plates of the DIMM power planes. This parallel LC circuit has an impedance peak at the resonant frequency $f_0 = 1/(2\pi\sqrt{ESL\ Cap})$, where Cap is the capacitance of the power planes and ESL is the inductance we seek to measure. Figure 1 shows the impedance vs frequency of the bare fab power planes before and after they are shorted together. Capacitance of the power planes is determined by the impedance of the unshorted planes at low frequency and ESL is calculated from the peak frequency and capacitance. The power loop inductance of the connector is found to be 670 pH which gives 12 mOhms reactance at 2.9 MHz. With a safety margin, it is assumed that the mother board can supply power at or below the target impedance up to 1 MHz. This is the “power bandwidth” of the connector for this application and is the minimum frequency where the DIMM must meet the target impedance.

Another very important inductance for the DIMM PDS is the mounting inductance for capacitors. Inductance in the pads, vias and power planes highly influence the ESL of the mounted capacitor, which in turn influences the resonant frequency of the mounted capacitor. The inductance of the decoupling capacitor mounts are determined by shorting the pads in the same way that the connector inductance was determined above. The inductance

of decoupling capacitors as well as the connector is determined in Figure 1 and summarized in Table 1.

Capacitors – The DIMM connector inductance determines the amount of bulk capacitance required on the DIMM. Bulk capacitance on the Dimm is required to provide PDS current beginning at the frequency where the mother board can no longer supply it. The reactance of capacitance is *1/(jωC)*. By using the target impedance and the minimum frequency at which the DIMM is required to meet the target impedance, the bulk capacitance requirements of the DIMM are calculated, $Cap = 1/(2\pi\ f\ Z_t) = 13\,uF$. A similar calculation can be made to determine the amount of capacitance required on a memory chip to compensate for the package and PCB mounting inductance.

Discrete Ceramic capacitors are used to meet the 12 mOhm target impedance in the 1-100 MHz frequency range. A resistive (flat) profile is more desirable than an inductive or capacitive (sloped) profile. A resistive impedance will damp all resonances but a reactive profile may feed resonances with additional energy. Capacitors have been characterized and modeled in Spice [2]. Figure 2 shows the simulated and measured impedance profiles of several capacitor values and serves as a menu to choose from. The flattest PDS profile can be designed by using 3 capacitor values per decade (i.e. 10, 22, 47, 100 nF, etc). Two capacitors (i.e. 10, 33, 100 nF, etc) or one capacitor (i.e. 10, 100, 1000 nF, etc) per decade may be used but will not result in as flat of a PDS profile.

Figure 3 shows the single node SPICE analysis for the capacitor matrices given in Table 2. Single node means that the all capacitors have been hooked together in parallel between a single node and ground. One AC amp has been injected into that node and the frequency swept between 100 kHz and 1 GHz. It is seen from the figure that the simulated capacitors will maintain the PDS below the target impedance in the desired frequency range. By using more types of capacitors, it is possible to maintain a lower impedance profile for the least cost, but more capacitor part numbers leads to more manufacturing complexity.

Measured Results – A two port vector network analyzer (VNA) has been used to measure a transfer impedance vs frequency of a DIMM stuffed with capacitors at several positions on the DIMM [3]. The DIMM power planes are not solid but are very "cut up" as each layer is used for both wiring and power transfer. Vcc is on 3 of the 6 layers, Gnd is on two and Vref is on one layer. Numerous vias connect the Vcc planes together and the Gnd planes together. The length of the DIMM is separated into 11 nodes according to the natural divisions made by the 18 memory and 2 register chips, one chip on each side of the DIMM.

With normal PDS designs, the board is square or has a small aspect ratio. The DIMM is a notable exception in that the board is nearly 5 times longer than it is wide and the power planes do not cover the entire width of the board. Also, most normal designs have solid or only slightly cut up power planes. Good model to hardware correlation can usually be obtained with single node analysis up to the 100 MHz range because all components are basically in the same "square" of power plane material and the time delay across the board is not significant compared to the period of 100MHz. However, the DIMM is very different. The long, skinny, cut-up nature of the power planes make the two port measurements on the DIMM very position dependent, where on a normal board they are not (below 100 MHz). Figure 4 shows the measured S21 parameters which have been converted to Z21 by the formula $|Z_{DUT}| = 25 \cdot 10^{\frac{|S_{21}|}{20}}\ \Omega$ for several positions on the stuffed DIMM. Port 1 was always on the far left hand position on the board. Z21, Z31, Z41... are measured between node 1 and nodes 2, 3, 4... Most of the nodes had open decoupling capacitor positions that could be used for measurement, but a few did not. The measured nodes are shown. The farther the second port is from the first port, the lower the transfer impedance.

A low transfer impedance should not be interpreted as a low PDS impedance. The transfer impedance measurement is also referred to as insertion loss. It is a measurement of the amount of loss that occurs in a signal that is traveling between the two ports of a VNA. On a normal PDS with solid power planes and square geometry, there is not very much insertion loss between the two ports. But in the case of the DIMM, much signal is lost as the signal must pass through series inductance and past parallel capacitance (discrete decoupling capacitors) as it goes from one side of the DIMM to the other.

Multinode Analysis - Figure 5 shows an attempt to model the long, skinny, cut up power planes with transmission line segments. The impedance and delay of each transmission line segment is estimated from the physical dimensions of the power plane geometries on each PCB layer [4]. The transmission line segments divide the DIMM into 11 nodes which represent the measured nodes, just like the Z21 thorugh Z11_1 measurements. For simulation, 1 amp is forced into node 1 and the voltage is measured at each of the other nodes. The appropriate discrete decoupling capacitor models have also been attached to each node. The simulated transfer impedance is plotted in dashed curves next to the measured solid curves in Figure 4. Good model to hardware correlation is obtained. This simulation verifies the attenuation or insertion loss expected as the VNA port locations are separated on the DIMM.

The measured and simulated multinode results do not compare well with the target impedance and

simulated single node results. This is because the load is distributed among the 11 nodes in actual product operation but the ports are not distributed in 11 locations for the VNA measurements. The SPICE simulation model that generated Figure 4 was modified so that the 1 amp forcing function was distributed evenly to the nodes closest to the memory chip locations. Figure 6 shows the transfer impedance vs frequency after the load is well distributed on the DIMM as it is in normal operation. In this figure, the transfer impedance at each load point closely matches the desired target impedance. The connector inductance to the mother board has been added in this simulation.

Conclusion – A PDS has been designed for the JEDEC DDR2 DIMM so that each memory chip will see a sufficiently low impedance at it's power terminals. Discrete ceramic capacitors are used on the DIMM to keep it's impedance less than 12 mOhms in the 1-100 MHz frequency range. Below that frequency range, power is supplied from the mother board. Power must come from on-chip decoupling capacitance above that frequency range. Measured impedances match well with simulated impedances after DIMM power planes are included.

References

1) L.D.Smith, R.E.Anderson, D.W.Forehand, T.J.Pelc, T.Roy, "Power Distribution System Design Methodology and Capacitor Selection for Modern CMOS Technology," IEEE Transactions on Advanced Packaging, Vol.22, No.3, August 1999, P284.
2) L.D.Smith, D.Hockanson, K.Kothari, "A Transmission-Line Model for Ceramic Capacitors for CAD Tools Based on Measured Parameters" Proc 52nd Electronic Components & Technology Conference, San Diego, CA., May 2002. pp.331-336.
3) I. Novak, "Measuring Milliohms and PicoHenrys in Power Distribution Networks," Design Con 2000.
4) L.D.Smith, T.Roy, R.E.Anderson, "Power Plane SPICE Models for Frequency and Time Domains," IEEE Transactions on Advanced Packaging, August 2001, P277.

Structure			S21 (dB)	freq (MHz)	Cap (nF)	Ind (pH)
Bare Fab Plane Capacitance			-20.05	30.026	2.13	
Shorted Connector				133.160		670
Capacitor Pad Location	via type	Size		freq (MHz)		Ind (pH)
DRams	single, end	0402		147.698		545
bottom	double, end	0402		101.012		1164
edge right	single, end	0603		162.414		450
middle	quad	0805		138.436		620

Table 1: Summary of data used to find connector and decoupling pad mounting inductance.

Value	Dielectric	Size	SRF (MHz)	10 types	7 types	4 types
10 uF	X5R	0805	1.6	1	2	4
4.7uF	X5R	0805	2.3	1		
3.3uF	X5R	0805	2.8		2	
2.2uF	X5R	0805	3.4	2		
1.0uF	X5R	0603	5.0	3	4	8
470nF	X7R	0603	7.3	3		
330nF	X7R	0603	8.8		6	
220nF	X7R	0603	11	4		
100nF	X7R	0402	16	6	8	16
47nF	X7R	0402	23	8		
33nF	X7R	0402	28		13	
22nF	X7R	0402	34	9		
10nF	X7R	0402	50	9	11	18
total cost ($)				46 0.52	46 0.76	46 0.94

Table 2: Capacitor matrix chosen in single node analysis. Ten types of capacitors give the flattest impedance profile for the least cost.

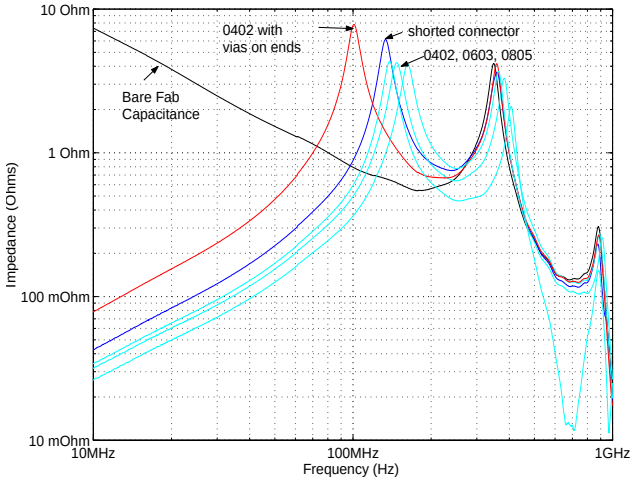

Figure 1: Shorted power planes are used to find inductance of the connector and capacitor mounts.

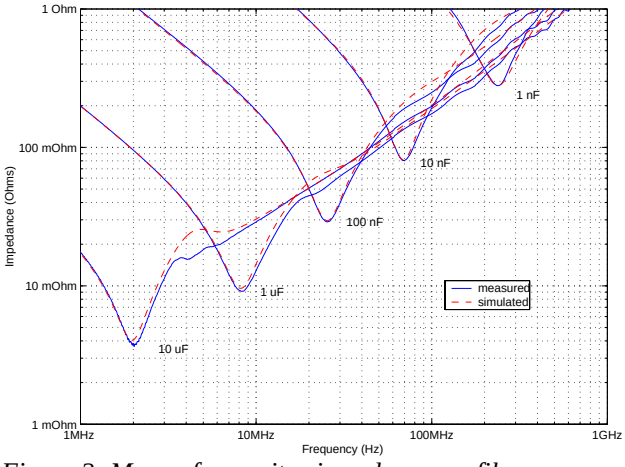

Figure 2: Menu of capacitor impedance profiles, measured and simulated.

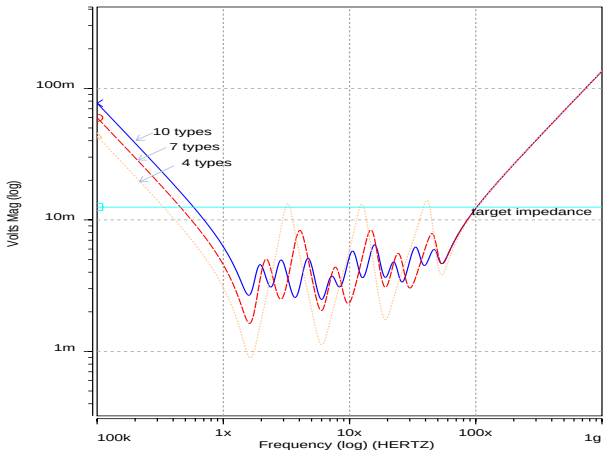

Figure 3: Single node SPICE analysis of 3 capacitor matrices compared to target impedance.

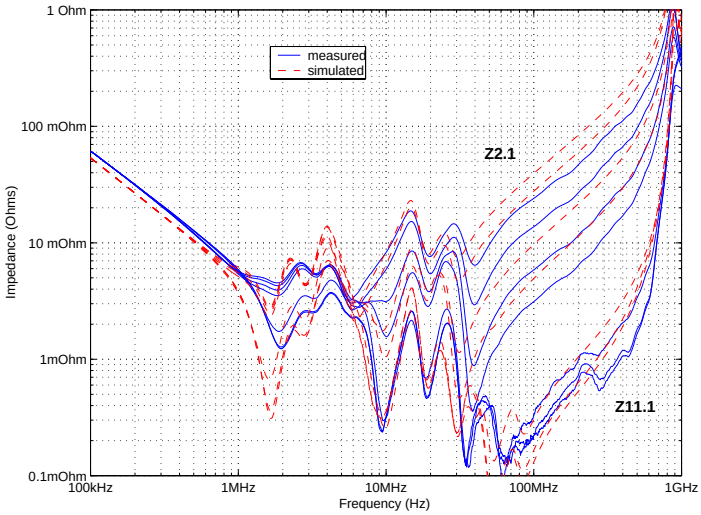

Figure 4: Measured DIMM impedance parameters compared with multinode simulation results. Transimpedance for the DIMM power planes is a strong function of probe position.

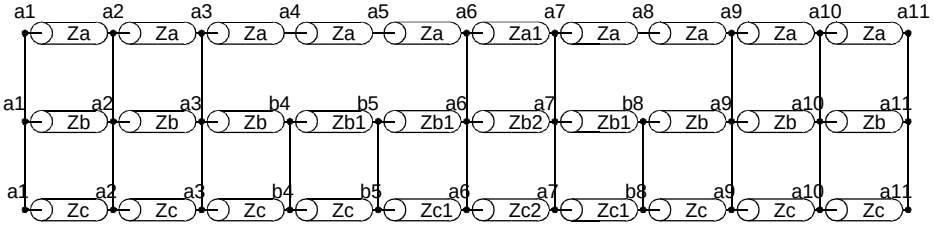

Figure 5: Transmission line representation of DIMM power planes. The DIMM is divided into 11 nodes.

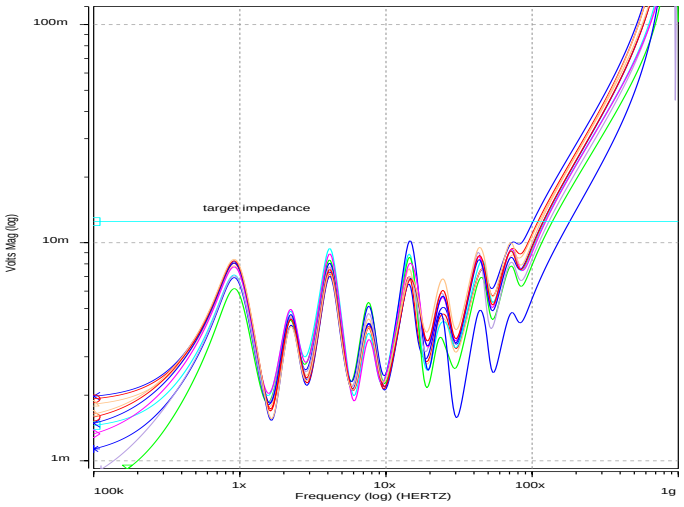

Figure 6: Multinode SPICE analysis with distributed loads. Each memory chip looks out and sees a PDS that meets target impedance.