Simultaneous Switch Noise and Power Plane Bounce for CMOS Technology

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Introduction

The simultaneous switch noise (SSN) problem has traditionally been thought of as an inductance problem. When many silicon drivers on a silicon chip switch at the same time, current crowds into the chip Gnd inductance or the Chip Vdd inductance. Ground bounce occurs that is proportional to the inductance in the ground or Vdd lead and the rate of change of current: V=L*di/dt. This line of thinking has been effective at solving SSN problems for traditional lead frame packages. Inductance matrices that account for the mutual inductance between signal, power and Gnd conductors are combined with silicon driver models in a circuit simulator to produce the expected noise waveforms for an SSN event.

But electronic packaging has progressed to packages that have power and ground planes. Traces in the packages behave more like transmission lines with impedance and delay rather than lumped inductors. The rise and fall time on the signal waveforms have gotten so fast that an edge may fit within the package. Wire bonds have been replaced by solder bumps and peripheral leads have been replaced by solder balls. The new structures may have less than 1/100 of the inductance of the electronic packages that we were using just a few years ago. The number of switching IO has increased from 10’s to 100’s and is approaching 1000.

Capacitive and resistive elements have been added to traditional inductance matrices to account for the time delay in the package and the losses. But the number of circuit elements in an SSN analysis and the increased number of simultaneously switching drivers have resulted in large, complex simulation runs that require much CPU time and computer resource. It has become harder and harder to get meaningful model to hardware correlation for the large SSN problem. It is time to consider a radically new approach to simulating the SSN problem.

Power Plane Bounce

The SSN problem has shifted from an inductance problem to a plane bounce problem. The major issue with modern SSN is managing the return current that occurs on the reference planes for signal transmission lines. The reference planes are not perfect and they bounce as return current accumulates and charges the parallel plate capacitance between power and Gnd planes.

The path that signal current takes in the electronic package and on the printed circuit board (PCB) is obvious: it follows the signal trace. But for every signal current, there is return current occurring somewhere in the system. In modern electronic packages, the return current is on a reference plane that is in close proximity to the signal trace. The plane may be at ground potential or it may be at some other (power supply) voltage. The reference plane controls the impedance of the trace. At reasonably high frequencies (more than 1 kHz), most return current for a transmission line travels on the nearest reference plane regardless of the direction of current on the trace. It matters not whether the signal transitions from high-to-low or low-to-high, the return current travels on the nearest reference plane.

This presents a problem at the 3 dimensional discontinuity at the end of a transmission line. Suppose the transition is from low to high and the cross-section of the package has the transmission line located above a Vdd plane as shown in figure 1. The driver connects the Vdd plane to the transmission line through a low impedance. Current flows from the Vdd plane onto the transmission line which is low, say ground potential. As the wave front propagates down the transmission line, charge flows into the capacitance between the trace and the Vdd plane, raising the potential on

the trace up to Vdd. The current path is complete because charge from the Vdd plane flows in a complete loop from the Vdd plane, through the driver and onto the transmission line that is referenced to the Vdd plane. If there is a ground plane underneath the Vdd plane, it is not disturbed because it is not part of the current loop.

But now, suppose that the driver switches from high-to-low on the same structure as shown in figure 2. The transmission line above the Vdd plane is initially charged at Vdd potential. The silicon driver connects the transmission line to the Ground plane through a low impedance. Current flows out of the transmission line, through the driver and onto the ground plane that is underneath Vdd. If current on the transmission line is flowing towards the driver, physics tells us that return current on the Vdd plane must be flowing away from the driver in the 2d transmission line cross-section. So far, we have an incomplete current path at the 3d discontinuity near the driver. Current is flowing from the driver onto the ground plane. Current is flowing away from the driver on the Vdd plane. The current path is completed through Vdd-to-Gnd decoupling capacitance in the vicinity of the driver.

Discrete decoupling capacitors are unable to respond at 1 nSec edge rates because of their series inductance [1]. Charge accumulates on the Vdd and Gnd planes, which behave much like the parallel plates of a capacitor. The equation Q=CV governs the situation and the power planes have a voltage bounce that is related to the capacitance between planes and the return current on the transmission lines. This is one of the major mechanisms that causes power plane bounce. The other is spreading inductance.

Model to Hardware correlation

Hardware has been built and measured that confirms that power planes bounce according to the return current on transmission lines. The hardware consisted of 4 very wide microstrip transmission lines that were approximately 22 Ohms. They were approximately 20 inches (50cm) long. The stackup was similar to figures 1 and 2. The power and ground planes were approximately 300 mils (7.6mm) wide and similar in length to the transmission lines. Due to the long thin nature of the power planes, they can also be modeled as single transmission lines. With the those dimensions and FR4 material, the power planes are modeled as 2.26 Ohm transmission lines. Four silicon drivers were located on the left side of the board with no power plane decoupling. Power was supplied to the right side of the board, which was well decoupled. The difference between Vdd and Gnd was measured on the left side of the board near the active drivers. Two experimental conditions were set up, one where the far ends of the transmission lines were open circuits and another where the far ends were terminated to both Vdd and Gnd with 44 Ohm resistors.

The discussion above predicts that much power plane bounce will occur in a high-to-low transition, but little power plane bounce will occur in a low-to-high transition. That behavior was observed in both lab measurements and spice simulation as shown in figure 3a and 3b. The power plane bounce was about 2 volts peak-to-peak. The circuit model is shown in figure 3c. Notice that spice node 0 is only on the right side of the board.

For the terminated case, a very different waveform was measured. The majority of power plane bounce was on the rising edge instead of the falling edge. This is predicted by the spice model. The measured data and simulation is in figure 4. Notice that at the instant the driver connects Vdd to the transmission lines, the Vdd voltage measured with respect to local ground jumps up more than a volt! This unexpected behavior is due to the initial conditions on the physical structures.

Prior to the low-to-high transition, current was coming from Vdd on the right side of the board, through the top 44 Ohm resistor in figure 4c, and down the 22 Ohm transmission line. The pull-down device in the driver conducted the current to local ground and where it returned back to the right side of the board on the 2.26 Ohm transmission line. With these initial conditions, the driver makes a low-to-high transition. Since the 22 Ohm transmission line is already energized with current, no pull-up device is necessary in the driver for the first several nSec. Current coming down the transmission line snaps the driver output high without any aid from the driver. Meanwhile, the 2.26 Ohm transmission line is charged with ground current. Magnetic flux within the transmission line wants to maintain a differential current in the transmission line. When the pull-down device in the driver becomes

high impedance, the current loop is opened up. Charge continues to leave the ground node of the driver, making it more and more negative with respect to Vdd. This explains why local Vdd bounces positive with respect to local Gnd at the driver position during a low-to-high transition in the terminated case.

Uncoupled transmission lines have been used to model the traces and power plane structures. This is justified by the skin effect and the superposition principles. For this experiment, solid copper power planes are 1.4 mils (35 μM) thick. The skin depth at SSN frequencies is much less than this. Return current occurs on the surface of the power plane that is closest to the trace. High frequency current on power planes is located on adjacent surfaces. Neither electric nor magnetic fields penetrate the solid copper planes, so the trace and power plane structures are electrically isolated from each other. The path that the trace takes above the copper plane is not important. The important considerations are the impedance, time of flight, start and end points of the transmission line. Charge is either removed from, or deposited on the power planes at the start and end points of the transmission line. This knowledge is used to greatly reduce the complexity of SSN simulation. The SSN problem is separated into a transmission line problem and a power plane problem. The problems are solved independently (uncoupled) and the solutions are superimposed back together.

This one-dimensional model to hardware correlation demonstrates the importance of power plane bounce in the SSN problem. Return current in the power supply path is responsible for the bounce. The same principles apply to a two dimensional printed circuit board (PCB). CPU run times are reduced from hours to minutes by eliminating almost all of the inductances and mutual inductances found in traditional SSN analysis.

Power Plane Model for SSN simulation.

As previously reported, power planes can be represented by an array of transmission lines [2]. The concepts demonstrated in the model to hardware correlation above apply to the 2 dimensional case. Spice has been used to simulate 100’s of simultaneously switching drivers inside an electronic package mounted on a PCB. The simulation included the inductance of the package solder bumps and solder balls and the effects of transmission lines referenced to bouncing power planes in both the electronic package and the PCB. The PCB was decoupled with about 100 decoupling capacitors and powered by a voltage regulator module (VRM) as described in [3]. The simulations indicate that the majority of SSN noise is due to power plane bounce. The SSN problem is changing from an inductance problem to a power plane bounce problem.

References

[1] T.Roy, L.D.Smith, "ESR and ESL of Ceramic Capacitor Applied to Decoupling Applications," IEEE Electrical Performance of Electronic Packaging Conference, Oct26, 1998.

[1] H.H.Wu, J.W.Meyer, K.Lee, A.Barber, "Accurate Power Supply and Ground Plane Pair Models," IEEE Electrical Performance of Electronic Packaging Conference, Oct 26, 1998.

[2] L.D.Smith, R.E.Anderson, D.W.Forehand, T.J.Pelc, T.Roy, "Power Distribution System Design Methodology and Capacitor Selection for Modern CMOS Technology," IEEE Transactions on Advanced Packaging, Vol.22, No. 3, August 1999.

Switch low-to-high

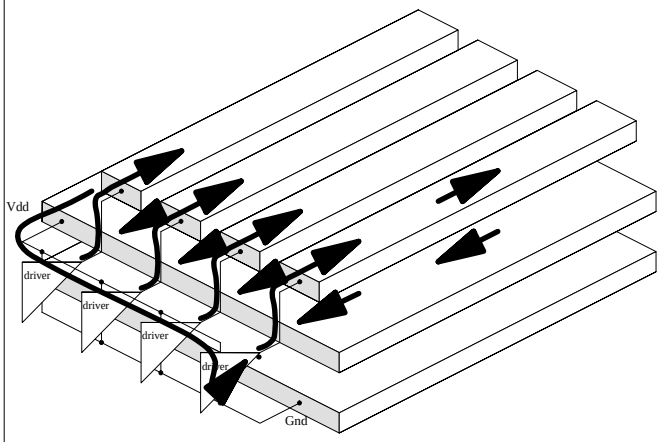


Figure 1

Switch high-to-low

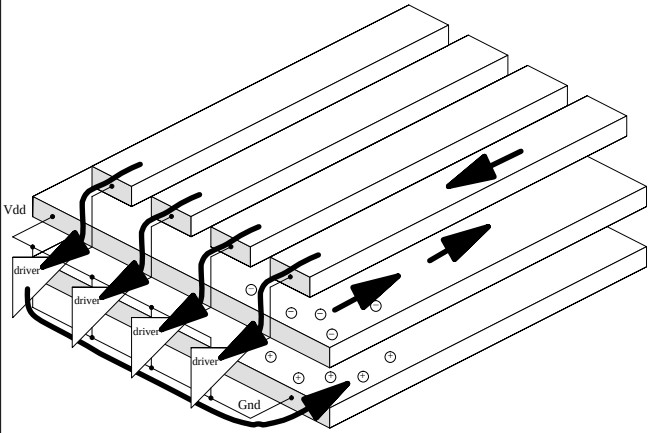
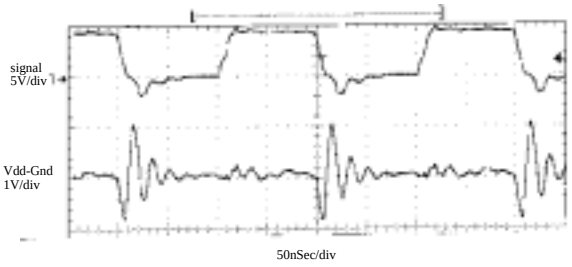


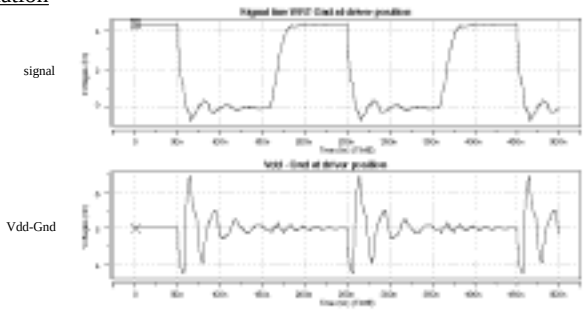
Figure 2

Figure 3: Open Circuit Termination

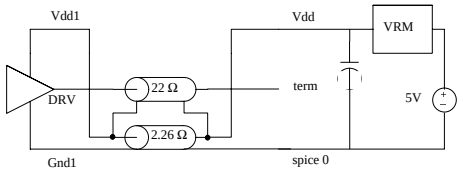
Measurement



Simulation



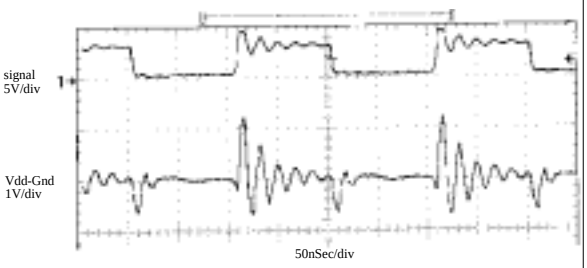
Simulated Model



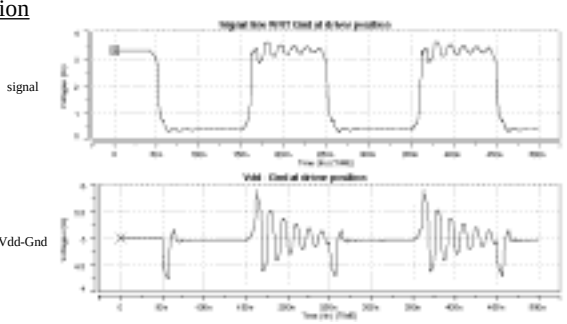
Rising edge produces little power supply noise.
Falling edge produces much power supply noise.
Falling edge requires displacement current between Vdd and Gnd planes.

Figure 4: Termination up and down

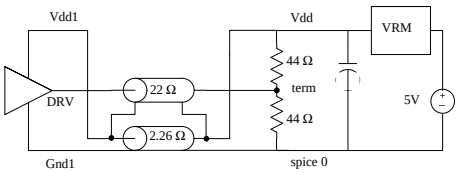
Measurement



Simulation



Simulated Model



Falling edge produces little power supply noise.
Rising edge produces much power supply noise.
Initial current is flowing _before_ the SSN event.