Decoupling Capacitor Calculations for CMOS Circuits

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Abstract— **CMOS circuits on printed circuit boards with continuous power planes require decoupling capacitors to keep power supply within specification, provide signal integrity and reduce EMC/EMI radiated noise. Capacitor values and quantities are calculated using time and frequency domain techniques.**

I. Introduction

The power supply for CMOS circuitry should be constant voltage and low impedance over a large range of frequencies. At low frequencies, the power supply specification is important because it is a factor in the speed and timing of logic circuits. It must be quiet near the clock frequency because many signals are taken in reference to it and noise on the power supply will reduce noise margin. High frequency noise produces common mode radiation from cables connected to circuit ground. Decoupling capacitance is the major consideration in controlling the impedance and noise on the Power supply.

Several authors have discussed the properties and usage of decoupling capacitors.[1,2,3] This paper first describes the properties of CMOS circuitry, electronic packages, printed circuit boards (PCBs) and decoupling capacitors that are used in modern electronic products. A complete solution to the decoupling capacitance problem must consider the properties of these system elements. A time domain method of calculating the decoupling capacitance required at the clock frequency is then demonstrated, given the average power dissipation of CMOS modules and the percentage ripple that can be tolerated on the power supply. Also calculated are impedance targets to be maintained over the entire frequency spectrum. Using frequency domain computer models, a circuit simulator is used to determine the decoupling capacitor values and quantity required at the PCB level to avoid problems with power supply specification, signal integrity and EMC/EMI.

II. Technology

CMOS logic technology will draw current when and only when the clock makes a transition. Some circuits draw current on both the up-going and down-going edges of the clock (i.e. clock tree) and other circuits draw current on just one edge (i.e. latches). Current flows from the chip Vdd node to the chip Gnd node every time an interior circuit makes a transition. This represents 80% of the power supply current for typical CMOS chips.[4] The remainder of the chip current is drawn by input/output (I/O) circuits. Current either comes from Vdd to charge up an I/O transmission line or is drawn out of an I/O transmission line and exits through chip ground. The majority of charge is drawn in a burst immediately after a clock edge with the lesser part of the charge drawn as transients die out on I/O transmission lines.

There is a variety of electronic packages for CMOS chips. Their electrical performance depends greatly on the presence or absence of a ground plane.[5] Those with a ground plane have much less power supply loop inductance (1 nH per Vdd/Gnd pair) than those without(10 nH per pair). Modern CMOS chips typically have ground plane packages to support the large number of I/O that are required to switch simultaneously. But this low loop inductance allows very fast current transients to reach the PCB power planes. The 'chip noise' that was once filtered out by the inductance of non ground plane packages now becomes a decoupling capacitance issue at the PCB level.

Printed circuit boards for modern CMOS chips have continuous Vdd and Gnd power supply planes. Their function is to deliver fast current transients to CMOS modules and provide a controlled impedance environment for high speed signals. The power planes form two plates of a capacitor and provide decoupling capacitance. Capacitance per area is calculated by

$$C_a = \frac{\varepsilon_r \varepsilon_0}{t}$$

where ε_0 is free space permiativity, ε_r is relative permiativity of the PCB dielectric and t is the thickness between planes. The inductance and impedance of the power planes are calculated by knowing the velocity which a plane wave would travel through the medium and the relationship between inductance, capacitance, velocity, and impedance.

$$vel = \frac{c_0}{\sqrt{\varepsilon_r}} = \frac{1}{\sqrt{L_a C_a}} \qquad Z_0 = \sqrt{\frac{L_a}{C_a}}$$

where c_0 is the speed of light in a vacuum, C_a is capacitance per area and L_a is inductance per square.

Calculated values for two power planes separated by 4 mils of FR4 dielectric ($\varepsilon_r = 4$) would be vel = 6 inches/nSec, Capacitance = 225 pF/inch^2, Inductance = 0.13 nH/square, Z_0 = 0.75 ohm-inch. A PCB 10 inches on a side will have capacitance 22.5 nF. The inductance in nH/square should be thought of similar to a spreading resistance (ohms/square) in a sheet of resistive material. A wave traveling down a long 10 inch wide strip of this medium will see 0.75/10 = .075 ohms of impedance. The above discussion is a direct application of field cell concepts presented by Kraus.[6]

Standing waves will exist at frequencies where an integer number of half waves fit on the PCB. The lowest frequency standing wave has wavelength

$$\lambda = 2 \times 10\ inches = \frac{\text{vel}}{\text{freq}}$$

In one dimension, a half wave will stand on the 10 inch PCB at 300 MHz. For decoupling capacitance considerations, the most important properties of the power planes are the capacitance and inductance, typically less than 1 nH between any two points of significant diameter.

Capacitors used for decoupling purposes are only capacitive at low frequencies.[7] At high frequencies, the capacitor becomes an inductor whose inductance is related to the path that current takes through the capacitor, almost as if it were made of a conductive material. Resonance occurs at the frequency predicted by

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

where L and C are the values of capacitance and inductance respectively. The impedance of the capacitor at resonance is the equivalent series resistance (ESR). A decoupling capacitor is modeled in a computer as a resistor, capacitor and inductor in series. The values of each are determined with an LCR bridge or by examining impedance vs frequency curves provided by capacitor manufacturers. A ceramic capacitor has a deep cusp at it's resonant frequency. A tantalum capacitor has a broad bottom or slope that different from one decade per decade.

III. Time Domain Analysis

Power supply current for a CMOS chip comes in spikes drawn shortly after the clock transitions as shown in Figure 1. Average power supply current is the time integral of charge through out the clock cycle. The charge drawn during a burst is

$$dQ = \frac{I}{2f_c} \text{ or } dQ = \frac{I}{f_c}$$

where dQ is the charge per burst and f_c is the clock frequency. The latter is true if most logic activity is initiated by latches triggered by one edge of the clock and the former is true if logic is triggered by both clock edges. The charge drawn by the chip will come from nearby decoupling capacitors and will reduce the voltage across the capacitor by

$$dV = \frac{dQ}{C}$$

where C is the decoupling capacitance. The amount of capacitance required to maintain the power supply to within some ripple specification is calculated by

$$C = \frac{dQ}{dV} = \frac{I}{2f_c \times Vdd \times n}$$

where Vdd is the power supply voltage and n is the fraction of ripple voltage allowed. Average current is found from average power which is usually known for thermal purposes.

$$I = \frac{P}{Vdd}$$

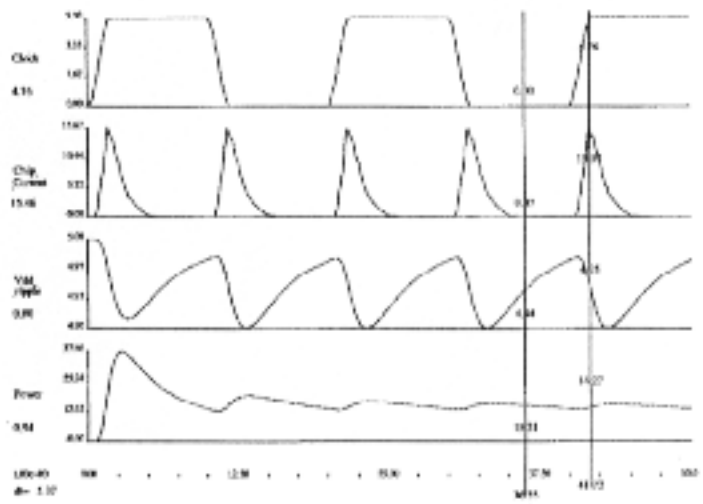

Figure 1. CMOS chip current is initiated by both edges of the clock. Decoupling capacitors supply the current but sustain a decrease in voltage resulting in Vdd ripple.

Table 1. Spread sheet calculations

Chip Name	Avg Pwr (watts)	Avg Current (amps)	Clock Freq (MHz)	Burst Charge (nCoul)	Cap req'd (nF)
CMOS ASIC 1	1.5	0.30	50	3.0	20.0
CMOS ASIC 2	3.5	0.70	50	7.0	46.7
CMOS ASIC 3	2.2	0.44	50	4.4	29.3
CMOS ASIC 4	4.3	0.86	50	8.6	57.3
CMOS ASIC 5	3.7	0.74	50	7.4	49.3
Total	15.2	3.04			202.7
Note: Vdd = 5 volts -- Ripple = 3% Ztarget = Vripple/Iavg = 49.3 mOhms Ztarget/2*Π 7.9 mOhms					

Table 1 shows spread sheet calculations for the decoupling capacitance required to maintain a 5 Volt supply to a 3% ripple specification given the average power for 5 ASICs on a PCB, assuming that current is drawn on both clock edges. If a CMOS chip has high and low power modes, then the high mode should be used for decoupling capacitance calculations. A target impedance is calculated by

$$Z_{target} = \frac{dV}{I} = \frac{Vdd \times n}{I}$$

The capacitance calculated by this method must be available at the clock and twice the clock frequency. Capacitors on their mounting pads must have resonance above those frequencies. The impedance of the capacitance calculated from burst current is

$$Z = \left| \frac{1}{j\omega C} \right|$$

where $\omega = 2\pi f$.

This yields a value that is $Z_{target}/2\pi$, which seems to be a contradiction. The capacitor impedance calculation assumes a perfect sinusoid at a frequency (i.e. 2x clock). But, the capacitance calculated from burst current assumes that all frequency components line up to produce a current spike. The maximum power supply impedance should be maintained below the upper limit. The impedance at the clock or 2x clock frequency should be at the lower limit. These limits are used in the frequency domain analysis.

IV. Frequency Domain Analysis

Computer models are assembled for all of the circuit elements that influence the power supply impedance. By forcing 1 amp of AC current through the elements and measuring the voltage across them, the impedance as a function of frequency is calculated by a circuit analysis program as shown in Figure 2. Many of the properties discussed in the technology section become apparent on these curves. At low frequencies, a ceramic capacitor is capacitive until resonance, after which it becomes inductive. All ceramics shown here had the same physical geometry and therefor similar inductances. A frequency dependant resistor has been used to accomplish the broad slope at the bottom of the 22μF tantalum curve. Also shown on the same plot is the output impedance of a switching power supply. It has high impedance after 100 kHz. The PCB power planes are high quality capacitance because the inductance is small. Impedance cusps occur as standing waves develop at frequencies above 300 MHz. These are the impedance characteristics of the components that make up a typical power supply for a modern CMOS product.

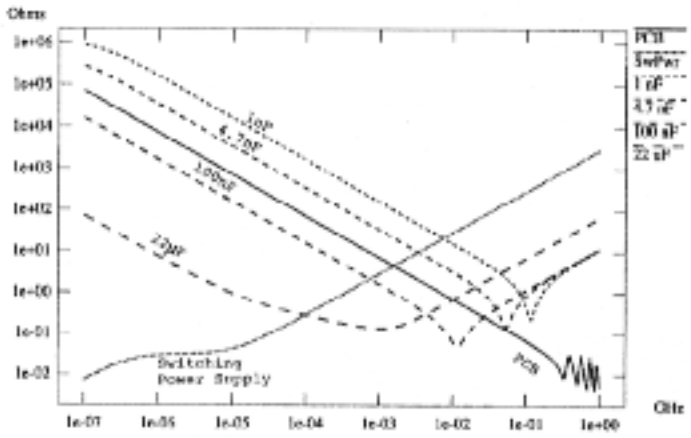

Figure 2. Impedance of individual components of power supply as a function of frequency

Figure 3 is a circuit diagram that shows power supply components in parallel. Again, if 1 amp AC is forced into the Vdd node with respect to Gnd, the voltage measured is the power supply impedance in Ohms. The PCB power planes have negligible inductance with respect to the vias that surface from the planes, wiring traces on top of the PCB and self inductance of capacitive components. The power supplies are considered to be singular nodes up to frequencies that produce standing waves on the PCB.

The circuit of Figure 3 is simulated with results shown in Figure 4. Several capacitors of the same value have been added in parallel as noted in the figure. They all have the same voltage across them, therefor conduct the same current. By trial and error, the quantity of each value capacitor was adjusted to bring the power supply impedance between the targets determined above. Adding capacitors of like value in parallel will reduce the power supply impedance in a frequency band near the resonant frequency for that value.

Other work has concluded that the addition of decoupling capacitors of different value does little to help high frequency performance.[8] The work assumed that a single capacitor of lessor value would be added to an existing capacitor to improve high frequency characteristics. An improvement of just 6 dB occurred above the resonance of the higher frequency capacitor (attributable to inductors in parallel). The present analysis is for many capacitors. As the quantities in Figure 3 suggest, an increasing number of capacitors is required as the capacitance value decreases (effectiveness frequency increases). The quantity of 1 nF capacitors could have been increased to bring the 200 MHz peak in Figure 4 below Z_{target}. The decision to do this involves a trade-off between manufactured cost and EMC emissions.

There are resonant peaks just as there are resonant valleys. A peak occurs at a frequency determined by the parallel combination of all the capacitors that have become inductive and the remaining capacitors that are still below resonance (capacitive). The most dangerous peak occurs just above the frequency where the lowest value capacitor resonates. The remaining capacitance is the PCB power planes which have very low inductance and ESR, almost 0. For this peak, there is not much resistance to reduce the quality factor of the resonant circuit. The best way to reduce the height of this peak is to minimize the inductance associated with the layout geometries that connect decoupling capacitors to the power planes.

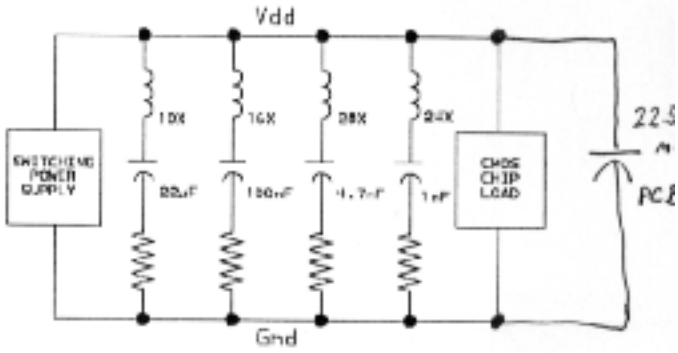

Figure 3. Circuit diagram showing quantity and value of decoupling capacities used on a 5 ASIC PCB

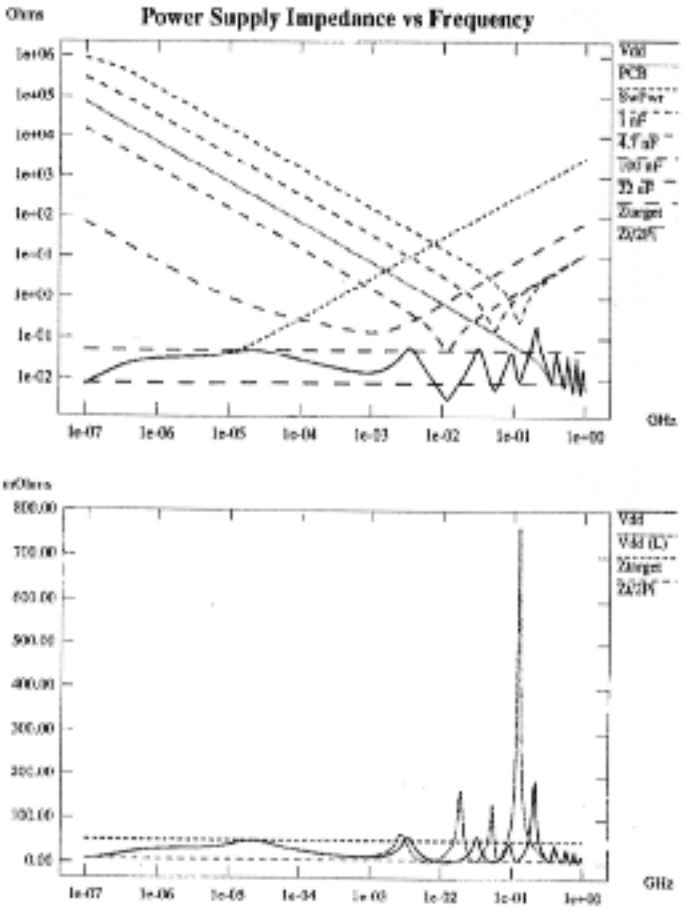

Figure 4. A. Power supply impedance vs frequency is shown on the solid line. For most frequencies, it is below the target impedance.
B. Same as Figure 4A but on a linear scale. Dotted line shows the result of mounting the same capacitors on inductive pads.

V. Layout

The geometries that connect surface-mount pads to power planes can easily dominate the inductance associated with a decoupling capacitor. Typical inductance for an 805 size (80x50 mils) capacitor is less than 1 nH and the PCB vias to the power planes are less than 1 nH if they are close enough together. A 200 mil trace of 6 mil wide copper that is 14 mils above a power plane is 2.5 nH. If two of them are used with a surface-mount pad as shown in Figure 5 the total loop is 5 nH. A better layout is shown in the same figure and is estimated to have 0.84 nH loop inductance. The dotted line in Figure 4B shows the impedance of the power supply when capacitors used in the previous analysis are mounted on the more inductive pads. Clearly, layout is important.

Figure 5. Surface mount pads for 805 size decoupling capacitors. Traces add much inductance.

As already discussed, the power planes are considered to be singular nodes at low frequencies and performance will not suffer if decoupling capacitors are placed anywhere on the PCB. However, differential mode EMI is proportional to loop area that radiating currents travel. Therefor, capacitors should be placed as close as possible to the CMOS chips that they are decoupling. Decoupling capacitors should also be placed at the edges of the PCB and near any connectors to backplanes or cables that leave the PCB. This is to prevent common mode radiation. Other work has suggested that decoupling capacitors should be distributed about the PCB to reduce radiation.[9] The distributed capacitors may be breaking up the PCB standing waves thereby reducing radiation.

VI. Summary

Decoupling capacitors are used to keep the power supply within specification at low frequencies, for signal integrity near the clock frequency and to reduce EMI radiation at high frequencies. Several values of capacitors are required to accomplish this. The capacitance required near the clock frequency is determined by time domain calculations and the capacitance required at other frequencies is determined by circuit simulation in the frequency domain. Target impedances for acceptable performance are calculated from chip power considerations. Layout for surface mount capacitors is critical in minimizing inductance and resonance at high frequencies.

VII. Acknowledgement

The author would like to thank Bill Wright for all of his helpful discussions on electronic packaging technology.

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