Model to Hardware Correlation for Power Distribution Induced I/O Noise in a Functioning Computer System

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Abstract

The Power Distribution System (PDS) for Input/Output (I/O) drivers in high-speed computer system is often separated from that for the microprocessor core. Modern computer systems contain hundreds of driver I/Os, decoupling capacitors and signal transmission lines that carry the data between chips. Simultaneous switching of these hundreds of drivers causes noise, i.e., voltage fluctuation on the power supply rail, which causes signal integrity problems of the data on the signal transmission lines. This paper discusses measurements of noise due to driver I/O switching in a high speed functioning computer system. Transfer impedance of PDS was measured and noise of functioning PDS in both frequency and time domain was measured. This paper presents an efficient methodology to model these noise waveforms. Modeling results have shown good agreement with measurements, demonstrating the application of the methodology to complex and realistic boards. Reduction of I/O switching noise through thin dielectric was also simulated using the modeling method presented.

Introduction

In a realistic system, the noise voltage generated by the simultaneous switching of N output drivers is given as [1]

$$\Delta V = N L_{eff} \frac{\Delta i}{\Delta t} \qquad (1)$$

where L_{eff} is the effective inductance of the power distribution system which accounts for all the parasitic inductance along the current path in the package, $\Delta i/\Delta t$ is the peak rate of change of current, Δi is the current required by each driver during the switching event, and Δt is the rise or fall time of the signal. Thus, the magnitude of the noise is proportional to the total power supply slew rate of the driver and the effective inductance of the power supply path. To meet the low inductance requirement, solid planes, which have the least inductance and resistance, are used for supplying power and ground in modern computer system [2].

A plane pair, which consists of two planes (say Vdd and Gnd) separated by an insulator, behaves as a cavity resonator at high frequencies. When circuits such as output drivers switch, return currents on reference planes deposit a time varying charge which result in a displacement current source in the cavity [3]. This current source excites radial electromagnetic waves in the cavity that reflect from the edges of the planes, causing multiple resonances in the cavity [4]. Depending on the impedance profile of the cavity, which can contain multiple resonances, the plane can bounce causing voltage fluctuations on the power supply rails of the chip. A measurement and modeling method for switching noise for output drivers driving transmission lines in a multi-layered functioning board containing planes has been described in this paper. The modeling method has been utilized for evaluating the switching noise for different dielectric thickness for reducing the switching noise.

Description of a Functioning System

The system includes 750 MHz microprocessors, heat sink, hundreds of driver I/Os, eight SRAMs and two connectors, as shown in Figure 1.

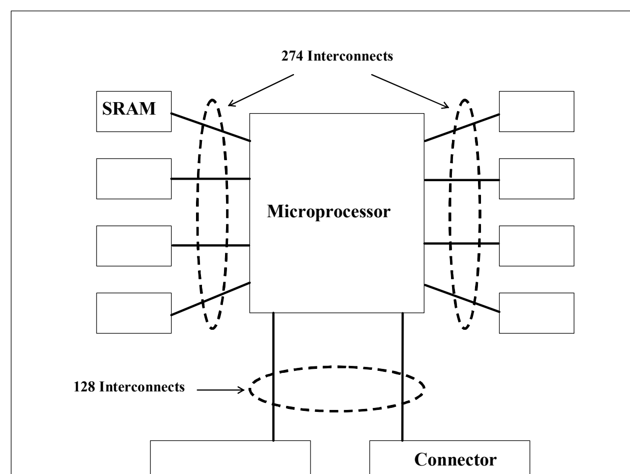


Figure 1. Top view of functioning board

The PDS for the driver I/Os in the system contain eight layers that were used for signal transmission lines. These transmission lines were driven by 402 drivers and include 274 transmission lines between microprocessors and SRAMs and 128 transmission lines between microprocessors and connectors. There were three vdd planes and three gnd planes, where all vdd planes and gnd planes were connected together to have the same dc level. The length of the planes was 9.44 inches and the width of the planes was 4.13 inches. The dielectric used between the planes was FR4. A total of 178 decoupling capacitors were distributed between I/O vdd and gnd planes. They have twenty different values of capacitance, equivalent series inductance (ESL) and equivalent series resistance (ESR). The resonance frequencies for these decoupling capacitors varied from 330 KHz to 1.5 GHz. The cross section of the system is shown in Figure 2.

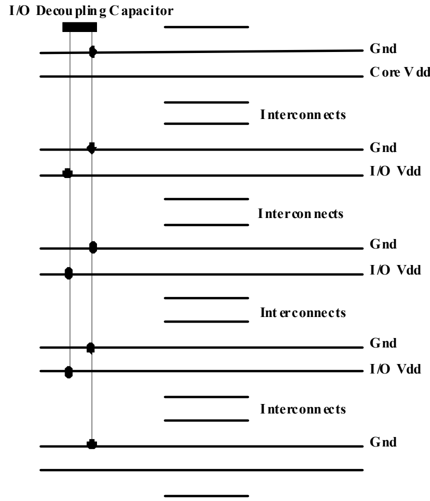


Figure 2. Cross Section of the functioning board

Measurements on a Functioning System

Measurements were conducted on a functioning computer system with 750 MHz microprocessors. The transmission coefficient from Port 1 to Port 2, S21, of the I/O vdd/gnd planes was measured as shown in Figure 3 using a vector network analyzer (VNA).

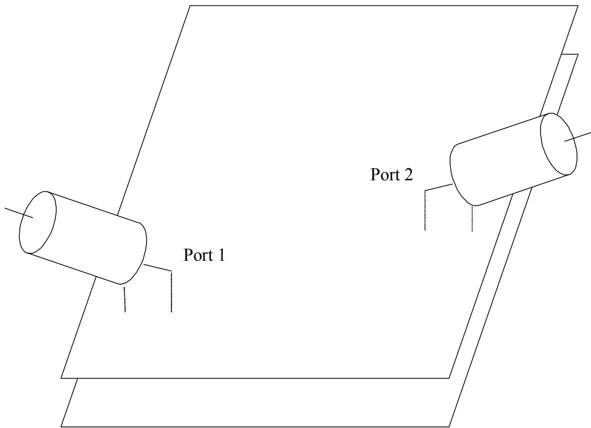


Figure 3. Measurement of vdd/gnd planes using VNA [5]

The VNA was calibrated by connecting the 50 ohm coaxial transmission lines associated with Port 1 and Port 2 together and doing a "through" calibration which was set as the reference level of 0 dB. The transmission lines were then soldered to vias connected to the vdd/gnd planes. The transfer impedance, Z_{trans}, was calculated from the magnitude of S21 (in dB) from [5]

$$|S_{21}| = 20\log_{10}^{\frac{|Z_{trans}|}{25ohms}} \quad and \quad |Z_{trans}| = 25 \bullet 10^{\frac{|S_{21}|}{20}} \qquad (2)$$

Figure 4 shows the transfer impedance of I/O vdd/gnd planes from the above measurement.

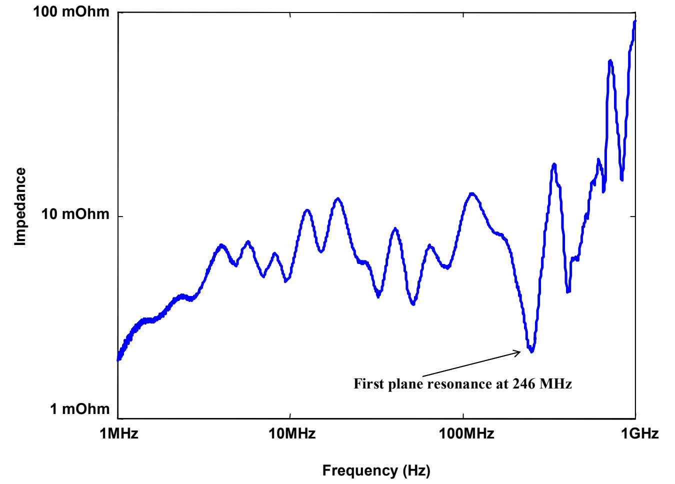


Figure 4. Measured transfer impedance of I/O vdd/gnd planes

178 decoupling capacitors, which were connected in parallel to vdd/gnd planes using the methodology in [6], enabled the planes to maintain a transfer impedance of about 10 mOhm upto 300 MHz. As shown in Figure 4, the first plane resonance occurs at 246 MHz. The resonances below that frequency are due to inductance and capacitance of the discrete decoupling capacitors.

A spectrum analyzer was used to measure the noise on the functioning board in the frequency domain. The 750 MHz microprocessors were functioning by getting power from the core vdd/gnd planes, which were isolated from the I/O vdd/gnd planes. They were fully stressed by software. 402 drivers were functioning by getting 1.5 V from I/O vdd/gnd planes. 274 of them were driving the transmission lines with a bus frequency of 250 MHz between the microprocessors and SRAMs. 128 of them were driving the transmission lines with a bus frequency of 125 MHz between the microprocessors and connectors, as shown in Figure 1. These transmission lines were located between the I/O vdd and gnd planes. The spectrum analyzer was set in "Max Hold" mode to record the maximum noise that occurred and the noise on the I/O vdd/gnd planes was measured. These results are shown in Figure 5.

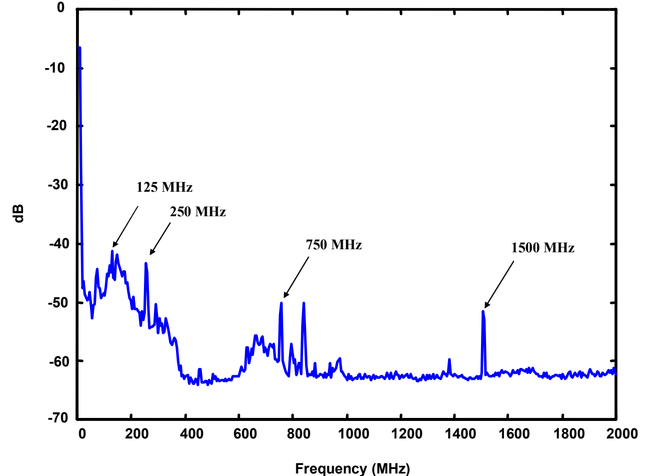


Figure 5. Measured noise of functioning board in the frequency domain

As shown in Figure 5, there are noise peaks at 750 MHz, which is the clock frequency of the microprocessor and at 1500 MHz, which is twice the clock frequency of the microprocessor. However, the maximum noise occurred at 125 MHz and 250 MHz, which are the bus frequencies of the connector bus and SRAM bus, respectively.

In packages containing planes, the return current is on a reference plane that is in close proximity to the signal transmission line. This is because at high speed, the return current follows the path of least inductance, not the path of least resistance. The lowest inductance return path lies directly under/above a signal conductor, minimizing the total loop area between the outgoing and returning current paths [7]. Thus, the transmission lines, which were embedded between the I/O vdd and gnd planes, reference both vdd and gnd planes while carrying the signal. The reference planes of the transmission lines are not perfect and they bounce as return currents from the transmission lines accumulate and charge the parallel plate capacitance, causing waves to propagate between the vdd and gnd planes [3], [4]. This is the reason why the noise at the bus frequencies are dominant on the I/O vdd/gnd planes, as shown in Figure 5.

The power distribution induced I/O noise in the time domain was measured using an oscilloscope. Figure 6 shows the result. The return currents on the reference planes accumulate time-varying charges, which act as a vertical current source. The radial electromagnetic wave excited by this current source causes the vdd/gnd planes to bounce, resulting in voltage fluctuation on the I/O vdd/gnd planes [3], [4] as shown in Figure 6.

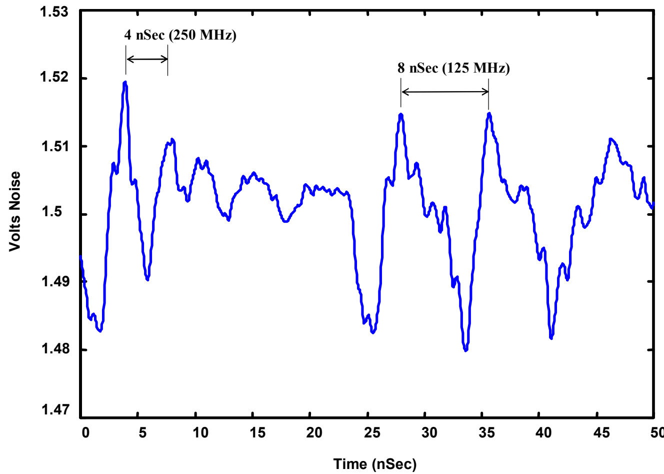


Figure 6. Measured noise of functioning board in the time domain

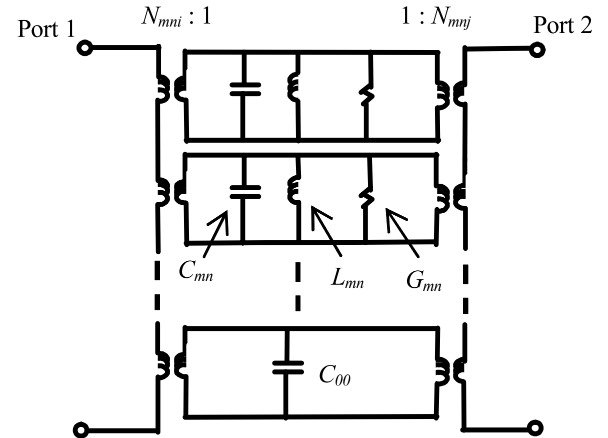
Maximum peak to peak noise (V_{pp}) voltage of 40 mV was measured when 402 drivers were switched simultaneously. It can be also reasoned in Figure 6 that the 4 nSec periodic noise is due to the SRAM bus which carried the signal at 250 MHz and the 8 nSec periodic noise is due to the connector bus which carried the signal at 125 MHz.

In this section, measurements conducted on the functioning board were described. Both frequency and time domain measurements indicate that I/O switching noise is caused by the return currents flowing on the I/O vdd/gnd planes. A modeling method which captures this effect will be discussed in the following section.

Modeling Methodology

There are three important components necessary to model the I/O switching noise on vdd/gnd planes of the functioning system described in the previous sections. These include planes, transmission lines and decoupling capacitors. The method to model each of these components will be discussed in this section.

The vdd/gnd plane is a critical component which needs to be modeled correctly since it is the reference conductor on which the return current of the signal line flows. The modeling method in [4] was applied to model the planes. Since the vdd/gnd plane pair acts as cavity resonator at high frequencies, it uses the equivalent circuit expressed in terms of *C*, *L* and *G* parameters, whose values are directly derived from the analytical expression in [8]. As shown in Figure 7, the capacitor '*C*' is used for storage of electric energy and the inductor '*L*' for storage of magnetic energy, whereby at the resonant frequency, there is an exchange of energy between the two elements, which forms a resonator circuit. The conductance '*G*' is used in the circuit to account for the losses both in conductor and dielectric.



$$N_{mni} = \varepsilon_m \varepsilon_n \cos\frac{m\pi x_i}{a}\ \mathrm{sinc}\frac{m\pi t x_i}{2a}\ \cos\frac{n\pi y_i}{b}\ \mathrm{sinc}\frac{n\pi t y_i}{2b}$$

$$N_{mnj} = \varepsilon_m \varepsilon_n \cos\frac{m\pi x_j}{a}\ \mathrm{sinc}\frac{m\pi t x_j}{2a}\ \cos\frac{n\pi y_j}{b}\ \mathrm{sinc}\frac{n\pi t y_j}{2b}$$

$$C_{mn} = \frac{\varepsilon ab}{d}$$

where

$$L_{mn} = \frac{d}{\varepsilon ab\,(2\pi f_{mn})^2}$$

$$f_{mn} = \frac{\sqrt{(m/a)^2 + (n/b)^2}}{2\sqrt{\varepsilon\mu}}$$

$$G_{mn} = \frac{2\pi f_{mn} C_{mn}}{Q_{mn}}$$

where

$$Q_{mn} = \frac{d\sqrt{\pi f_{mn} \mu\sigma}}{1 + d \tan\delta \sqrt{\pi f_{mn} \mu\sigma}}$$

Figure 7. Equivalent circuit for a plane pair [4]

The information on the "port" is captured by N_{mni} and N_{mnj} which are the ideal transformer turn ratio for the port *i* and *j*, respectively. Therefore the equivalent circuit in Figure 7 models the plane pair as a waveguide that is coupled to the various natural modes of the resonators through transformers. Based on the physical parameters such as width and length of the plane (a and b), dielectric thickness (d), permittivity and permeability of the dielectric (ε and μ), loss tangent of the dielectric ($tan\delta$), conductance of the plane (σ) and port location and size (x_i, y_i and t_{xi}, t_{yi}), the circuit for the planes can be constructed and ready for incorporating other components. The accuracy of the model has been demonstrated through experiments in [4]. In the functioning board, there were three vdd planes and three gnd planes, where all vdd planes and gnd planes were connected together to have the same dc level. These three plane pairs have been treated as one plane pair by using one third of the dielectric thickness in the modeling to reduce the size of the circuit.

402 transmission lines with Z_0 of 50 ohm were located between the vdd and gnd planes as shown in Figure 8. In the figure, *d1* is the distance between signal trace and vdd plane and *d2* is the distance between signal trace and gnd plane. When the currents from the driver flow on the transmission lines, the return currents flow both on vdd and gnd planes.

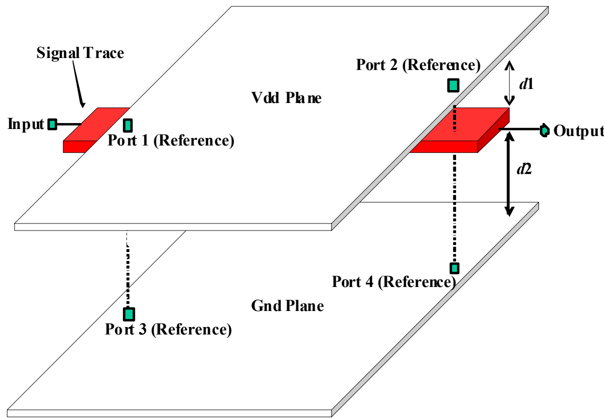


Figure 8. Transmission line between vdd/gnd planes

To account for the return currents in the above structure, the transmission line can be modeled using a skin effect approximation as in Figure 9, where the references for the transmission line are both vdd and gnd planes.

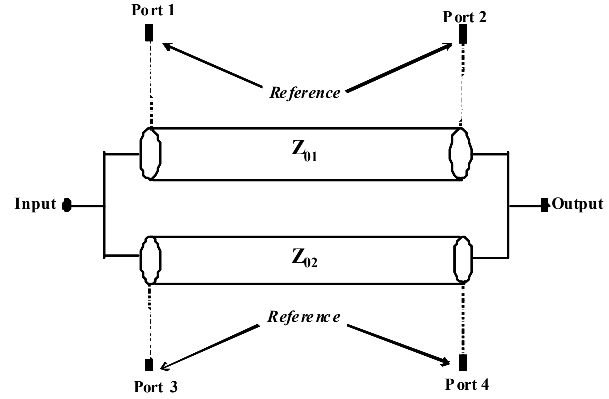


Figure 9. Equivalent circuit for transmission line

As shown in Figure 9, two transmission lines in parallel, each with a different characteristic impedance, can be used for referencing the vdd and gnd planes. The characteristic impedance of the transmission lines in Figure 9 are given by:

$$Z_{01} = Z_0 \frac{d1 + d2}{d2} \quad (3)\text{ a}$$

$$Z_{02} = Z_0 \frac{d1 + d2}{d1} \quad (3)\text{ b}$$

The model used in Figure 9 ensures that the magnetic field produced by the signal line is contained between the transmission line and the corresponding plane, which is valid at high frequencies. When *d1* is equal to *d2*, two transmission lines in parallel, each with twice the impedance of Z_0, can be used. Twelve transmission lines, including 8 transmission lines from SRAM buses and 4 transmission lines from connector buses, were selected for simulation. The characteristic impedance of the transmission lines were scaled down accordingly. The circuit model for the transmission lines were incorporated into the circuit model for the planes described earlier.

There were 178 decoupling capacitors distributed between I/O vdd and gnd planes, whose resonance frequencies varied from 330 KHz to 1.5 GHz. The measured values of capacitance, ESL and ESR were used for the construction of series RLC circuit for the capacitors.

It should be mentioned that when the equivalent circuit for a vdd/gnd plane pair, in Figure 7, is generated, all the necessary "ports" should be generated as well. These ports were determined by the position of the power supply, local driver vdd and gnd, transmission line references and decoupling capacitor locations. This information can be obtained from the physical layout of the board.

The modeling methodology for the functioning system employs superposition of circuit models for planes and transmission lines described in this section based on skin depth approximation to account for the return currents correctly. Simulation results based on the modeling method are correlated with measurements in the next section.

Model to Hardware Correlation

The equivalent circuit for vdd/gnd planes in Figure 7 with 178 decoupling capacitors at their corresponding locations was stimulated using a 1 Amp current source and simulated in HSPICE. Figure 10 shows the comparison between simulated transfer impedance and VNA measurements.

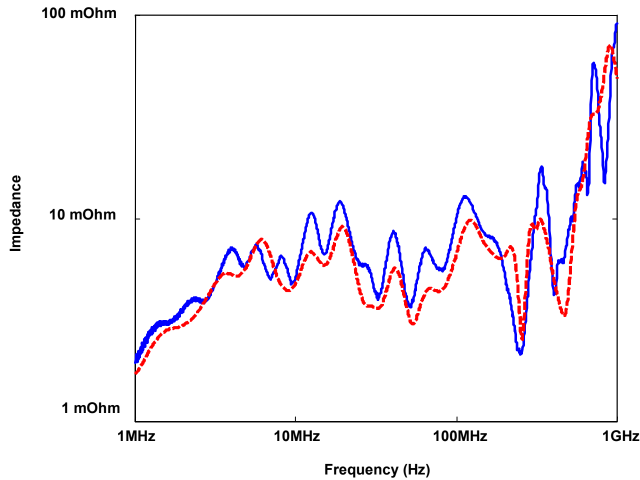


Figure 10. Model to hardware correlation for transfer impedance: Dashed (Simulation), Solid (Measurement)

The models for the transmission lines, drivers and power supply were incorporated and the entire circuit was simulated in the time domain. Figure 11 shows the simulated switching noise on the I/O vdd/gnd planes compared with the oscilloscope measurements. The CPU time required for time domain HSPICE simulation was 124 Seconds with 20 pSec time step for 50 nSec duration.

Both frequency and time domain simulation show good model to hardware correlation, demonstrating the application of the methodology for modeling complex and realistic system level boards.

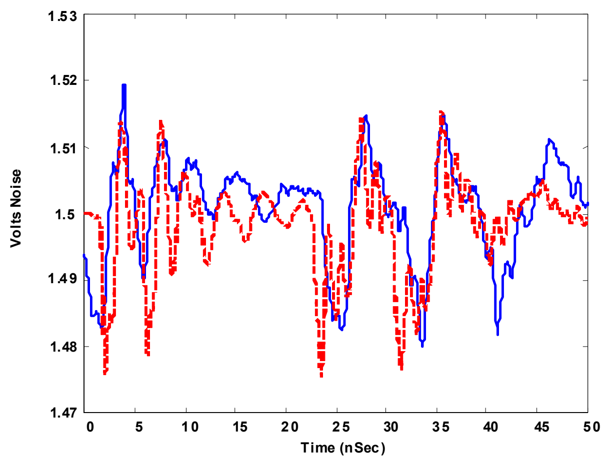


Figure 11. Model to hardware correlation for I/O noise: Dashed (Simulation), Solid (Measurement)

Reduction of I/O Noise Through Thin Dielectrics

The modeling method described in this paper has been used to evaluate the effects of dielectric thickness on the reduction of I/O noise. In the PDS where the planes are used for supplying power and ground, I/O switching noise can be reduced if enough attenuation is provided to suppress plane resonances. The attenuation in dB can be expressed as [9], [10]

$$A^{dB} = 4.35\left(\frac{R_s}{Z_0} + G_d Z_0\right) \qquad (4)$$

where Z_0 is the characteristic impedance and R_s and G_d are the series resistance of the conductor and parallel conductance of the dielectric, respectively. The above expression states that the same series resistance produces higher attenuation if the characteristic impedance is lower. The characteristic impedance of the plane pair is given as $Z_0 = \sqrt{L/C}$. Thus, with tightly spaced power planes, capacitance (C) increases and inductance (L) decreases, resulting in a low characteristic impedance.

Figure 12 (a), (b), (c) shows time domain simulation results for the same functioning board with dielectric thickness of 2, 1 and 0.5 mils, demonstrating the effectiveness of thin dielectric for reducing I/O switching noise. Peak to peak noise (V_{pp}) has been reduced from 39.9 mV to 15.8 mV by replacing 2 mil thick dielectric with 0.5 mil thick dielectric, as shown in Figure 12.

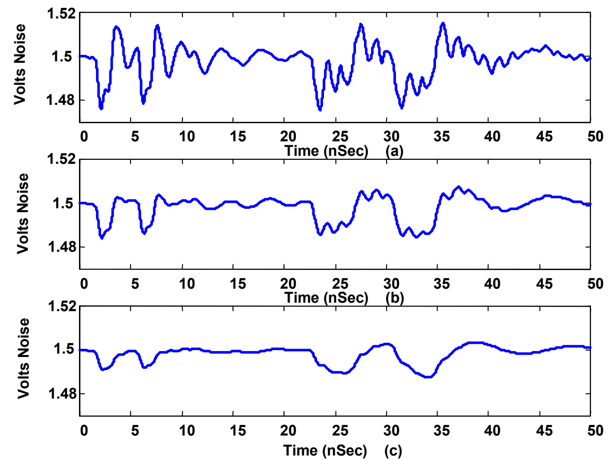


Figure 12. Simulated I/O noise for different dielectric thickness: (a) 2 mils: V_{pp}=39.9 mV (b) 1 mil: V_{pp}=23.4mV (c) 0.5 mil: V_{pp}=15.8 mV

Conclusions

Measurements conducted on the functioning I/O PDS were discussed in this paper. Both frequency and time domain measurements indicate that I/O switching noise is caused by the return currents flowing on the I/O vdd/gnd planes. Efficient method to model the I/O switching noise on a functioning system board was described, which accounted for the return currents correctly. Modeling results have shown good agreement with measurements, verifying the validity of the modeling methodology. Simulation also demonstrated that I/O switching noise can be reduced by using thin dielectric, which provides the attenuation to suppress the plane resonances.

References

1. William D. Brown, Advanced Electronic Packaging, IEEE Press (1998), Chapter 3.
2. Barry J. Rubin, "Comparison of Mesh and Solid Planes for Use in Electrical Packaging," *IEEE 5th Topical Meeting on Electrical Performance of Electronic Packaging*, 1996, pp. 217-219.
3. Larry Smith, "Simultaneous Switch Noise and Power Plane Bounce for CMOS Technology," *IEEE 8th Topical Meeting on Electrical Performance of Electronic Packaging*, San Diego, CA, October. 1999, pp. 163-166.
4. Sungjun Chun, Madhavan Swaminathan, Larry D. Smith, Jegganathan Srinivasan, Zhang Jin and Mahadevan K. Iyer, "Modeling of Simultaneous Switching Noise in High Speed Systems," *IEEE Transactions on Advanced Packaging*, Vol. 24, No. 2 (2001), pp. 132-142.
5. Larry D. Smith, David Hockanson, "Distributed SPICE Circuit Model for Ceramic Capacitors," *Proc 51th Electronic Components and Technology Conf*, Orlando, FL, May. 2001, pp. 523-528.
6. L. D. Smith, R. E. Anderson, D. W. Forehand, T. J. Pelc, T. Roy, "Power Distribution System Design Methodology and Capacitor Selection for Modern CMOS Technology," *IEEE Transactions on Advanced Packaging*, Vol. 22, No. 3 (1999), pp. 284-291.
7. Howard Johnson, Martin Graham, High-Speed Digital Design, Prentice Hall (1993), Chapter 5.
8. T. Okoshi, Planar Circuits for Microwaves and Lightwaves, Springer-Verlag (1985), Chapter 2.
9. I. Novak, R. E. Anderson, T. Roy, L. D. Smith, "Lossy Power Distribution Networks With Thin Dielectric Layers and/or Thin Conductive Layers," *IEEE Transactions on Advanced Packaging*, Vol. 23, No. 3 (2000), pp. 353-360.
10. Larry D. Smith, Raymond Anderson, Tanmoy Roy, "Power Plane SPICE Models and Simulated Performance for Materials and Geometries," *IEEE Transactions on Advanced Packaging*, Vol. 24, No. 3 (2001), pp. 277-287.