Published in Conference Record, Electrical Components Technology Conference
(ECTC), San Diego, CA, pp. 331−336, May 2002.

A Transmission−Line Model for Ceramic Capacitors for CAD Tools Based on Measured Parameters

Larry D Smith, David Hockanson, Krina Kothari
Sun Microsystems, Inc. MS MPK15−103
901 San Antonio Road, Palo Alto, CA, 94303−4900
Phone: 650−786−3303, FAX: 650−786−6457
larry.smith@sun.com, david.hockanson@sun.com, krina.kothari@sun.com

Abstract

An efficient and accurate transmission−line model for discrete MLC capacitors is developed. Hardware measurement techniques are used to obtain the circuit parameters for the model components. Low inductance measurement fixtures are required to observe and measure the transmission line parameters. The simulated impedance vs frequency results match closely with hardware measurements in the capacitance, resistance and inductance portions of the transfer impedance curve. The transmission−line model is well suited for CAD tools that are used to design power distribution systems.

Introduction

Discrete MLC (multi−layer ceramic) capacitors are commonly used in decoupling applications for computer systems. As the clock frequency and power consumption of micro processors continues to increase, it is important to provide low impedance power at high frequency. This is required to ensure reliable performance and compliance to world−wide electromagnetic−compatibility (EMC) standards [1][2]. CAD tools have been developed to assist in the design of power distribution systems [3]. The tools rely on accurate simulation models for all components of the power distribution system, including MLC capacitors.

Transmission−line models for capacitors have been previously described [4][5]. The traditional RLC model is inadequate for predicting the impedance of MLC capacitors at frequencies above series resonance. A transmission−line model may be used to provide increased accuracy for predicting the impedance of the board−level power−distribution system with simple circuit simulators [6]. A method for extracting circuit parameters from measurements for the transmission−line model is described herein. Common fixtures used by the capacitor industry for measurement are generally too inductive to yield results demonstrating the transmission−line nature of the capacitor. Through the use of a low inductance fixture, a vector network analyzer (VNA) is used to make S21 measurements which are converted to transfer impedance. The impedance at several points along the curve is used to determine the parameters for the MLC transmission−line model.

A MLC capacitor is shown in Figure 1. By inspection, the capacitor appears to be very similar to a parallel−plate transmission−line that is constructed with a serpentine geometry. Historically, the mounting inductance has masked the transmission−line nature of the capacitor. The high inductance forces the series resonance between the mounting inductance and capacitor to be below the resonance of the capacitor transmission−line. However, modern and next generation mounting technologies have pushed the mounting

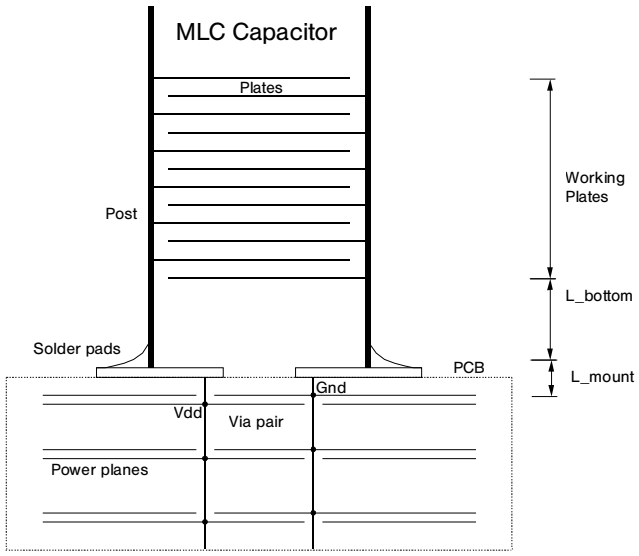

Figure 1: Construction of MLC capacitor mounted on PCB fixture. Inductance is associated with the working plates, the filler plate and the mount.

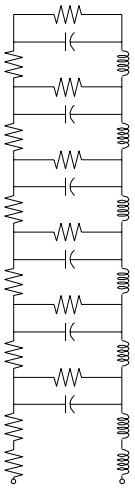

Figure 2: Traditional transmission line model topology.

inductance of high−density printed circuit boards (PCBs) to a small enough value to require a more accurate equivalent circuit model for capacitors. Accurate models can be used to shorten the design cycle and the cost of products by limiting the number of capacitors to the quantity that are absolutely required to meet the given design specification.

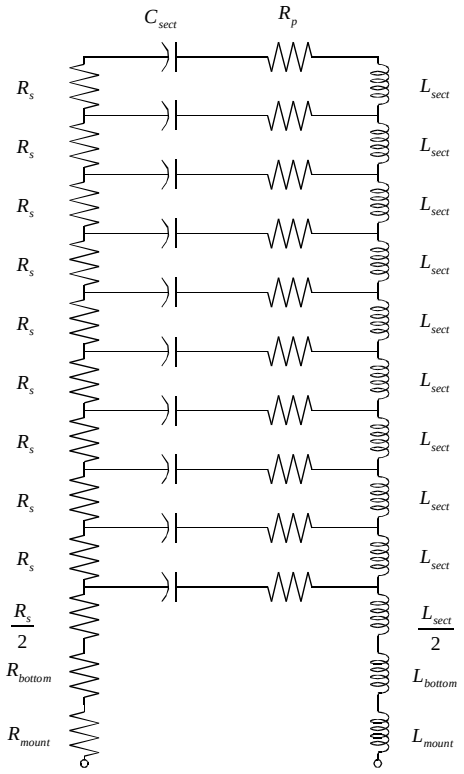

Figure 3: Transmission line circuit model for MLC capacitor.

Theory

The capacitor as depicted in Figure 1 should be very accurately modeled by the standard transmission−line equations given in frequency−dependent form by

$$\frac{d}{dz}V(z) = -(R + j\,\omega L)I(z) \quad \text{and} \qquad (1)$$

$$\frac{d}{dz}I(z) = -(G + j\,\omega C)V(z) \quad . \qquad (2)$$

These equations can be used to generate the per−unit equivalent circuit shown in Figure 2. Unfortunately, the resistance *R* and conductance *G* are typically functions of frequency [7]. Incorporating the frequency dependence into a circuit−simulation program is difficult and time consuming. However, for the frequency band that the capacitor is expected to be contributing to the power−distribution system, the model shown in Figure 2 may be modified.

The conductance and resistance parameters of the capacitor are expected to be inconsequential over bands remote from the resonances. Consequently, a loss in series with the capacitance for each section of transmission line can be used to approximate the frequency dependence in the parallel position of the circuit [7][8]. The resulting model is shown in Figure 3. The loss used in the modified model is essentially the average loss over the band of relevance, and can be chosen by following the measurement techniques detailed in the following sections.

Measurements

A simple coaxial probe test fixture is constructed to measure the transfer impedance of a SMT capacitor with minimal inductance. Flexible coaxial cables with SMA connectors are attached to Ports 1 and 2 of the VNA. The cables are soldered together to minimize the deviations from the 50 ohm line impedance of the cable as shown in Figure 4. A through calibration is performed which establishes the 0 dB reference level. Zero dB is equivalent to 25 Ohms because of the two properly terminated 50 Ohm transmission lines in parallel leading away from the test point. The DUT (device under test, capacitor) is then soldered in across the transmission lines forming a shunt impedance between the inner and outer conductors as shown in Figure 5 and 6. S21 parameters are measured and recorded. S21 is converted to impedance by using the equations:

$$|S_{21}| = 20\log_{10}\frac{|Z_{DUT}|}{25\,\Omega} \quad \text{and} \quad |Z_{DUT}| = 25\cdot 10^{\frac{|S_{21}|}{20}}\,\Omega \quad . \qquad (3)$$

The S to Z parameter conversions in Pozar [9] reduce to these equations when Z_{DUT} is much less than 25 Ohms.

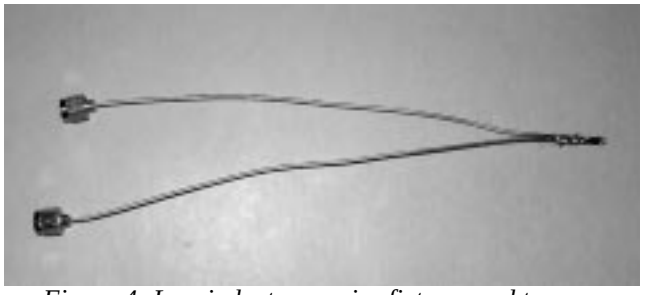

Figure 4: Low inductance wire fixture used to measure MLC capacitors.

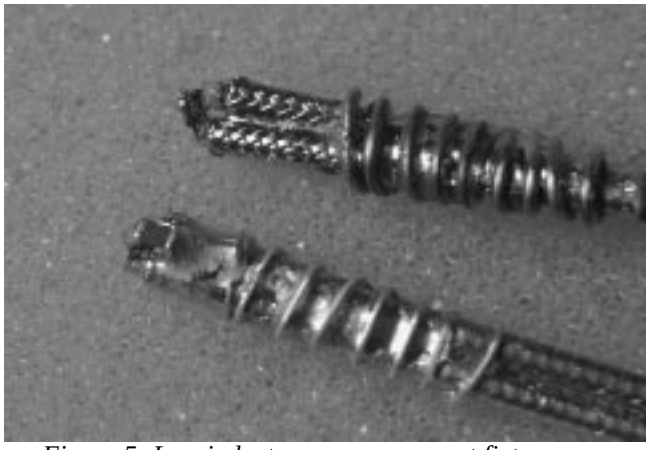

Figure 5: Low inductance measurement fixtures without (top) and with (bottom) a capacitor mounted as the DUT.

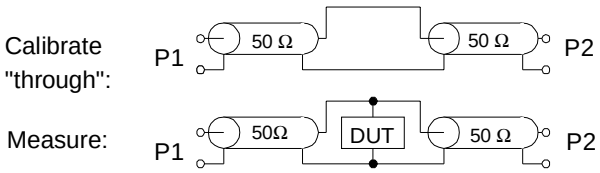

Figure 6: Schematic diagram of the calibration and measurement of the device under test (DUT, capacitor).

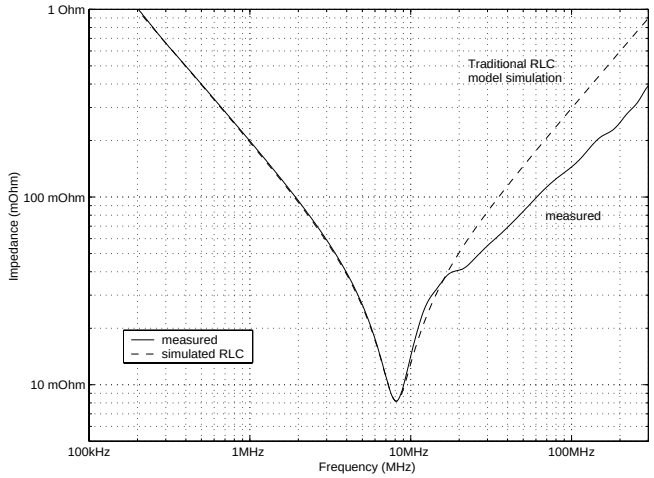

Figure 7: Measured and simulated results for 1 uF 0603 MLC capacitor. A series RLC model is simulated with R=8.2 mOhms, L=746 pH and C=801 nF.

A measured curve of impedance vs frequency is shown in Figure 7. The three distinct portions for the curve for capacitance, *ESR* (equivalent series resistance) and inductance are readily identified in the −20dB/decade, minimum and +20 dB/decade sections respectively.

The capacitance value is obtained by picking an impedance point on the capacitive portion of the curve and using the equations

$$|Z| = \frac{1}{|j\,\omega\,Cap|} \quad \text{and} \quad Cap = \frac{1}{2\,\pi\,f\,|Z|} \quad , \tag{4}$$

where f is frequency and ω is radial frequency. *ESR* is the value of impedance at the minimum of the curve which occurs at series resonance. A series RLC circuit has resonant frequency

$$f_0 = \frac{1}{2\,\pi\,\sqrt{ESL \cdot Cap}} \tag{5}$$

where f_0 is the frequency at the minimum point of the curve. *ESL* (equivalent series inductance) is then calculated from capacitance and resonant frequency

$$ESL = \frac{1}{Cap \cdot (2\,\pi\,f_0)^2} \quad . \tag{6}$$

Capacitance, *ESR* and *ESL* are extracted from the measured impedance curve in this manner and are 801 nF, 8.2 mOhms and 476 pH for the curve in Figure 7.

SPICE simulation of the simple RLC model for these parameters is also shown in Figure 7 next to the measurements. Good matching is obtained on the capacitive and resonance portions of the curve, confirming that the calculated values for *Cap*, *ESR* and *ESL* are correct. However at higher frequencies, the simulated and measured values depart. The apparent inductance at higher frequencies is obtained by picking an impedance point on the inductive portion of the curve and using the equation

$$|Z| = |j\,\omega\,L_{high}| \quad \text{and} \quad L_{high} = \frac{|Z|}{2\,\pi\,f} \quad . \tag{7}$$

By using a transmission−line model for the capacitor, it is possible for simulation to match measurements of the whole curve, including the high frequency section.

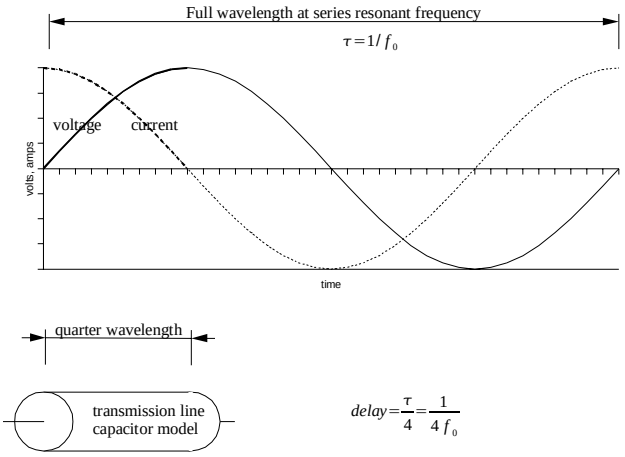

Figure 8: The Transmission line capacitor is a quarter wavelength long at series resonant frequency.

Capacitor Construction

The entire structure of Figure 1 is divided up into three parts: the working plates of the capacitor, the filler plate inside the capacitor and the mounting structure of the PCB. Intuitively, the transmission−line model may be partitioned into these three distinct regions and circuit parameters developed for each. Inductances are assigned to each of the three regions. *ESL* is the sum of these partial inductances. Let L_{cap} represent the inductance associated with with the working plates of the capacitor.

$$ESL = L_{mount} + L_{bottom} + L_{cap} \quad . \tag{8}$$

All three inductances contribute to the series resonant frequency of the capacitor. When mounting inductance and bottom inductance are minimized or eliminated, only the inductance associated with the plates of the capacitor is left. The internal plate inductance and capacitance of an MLC capacitor is well represented by a transmission−line model.

Circuit Model

It is necessary to find the parameter values for all components of the transmission−line model shown in Figure 3 in order to perform circuit simulation. The value for C_{sect} is simply the total measured capacitance divided by the number of sections, n.

$$C_{sect} = \frac{Cap}{n} \tag{9}$$

The inductance associated with the working plates is not as obvious but can be found from transmission line considerations. The capacitor is considered to be an open circuited transmission line. At series resonance, the transmission line is 1/4 wavelength long, forming a quarter wavelength resonator. The far end of the transmission line is open circuit, therefore high impedance. A low impedance is observed at the near end of the quarter wavelength transmission line at series resonance.

Figure 8 schematically shows a quarter wavelength transmission line resonator. The magnitude of the voltage and current standing waves along the length of the transmission line are shown in the dark portion of the curves. The lighter portion of the curves shows the length of a full wave at the frequency of quarter wavelength resonance,

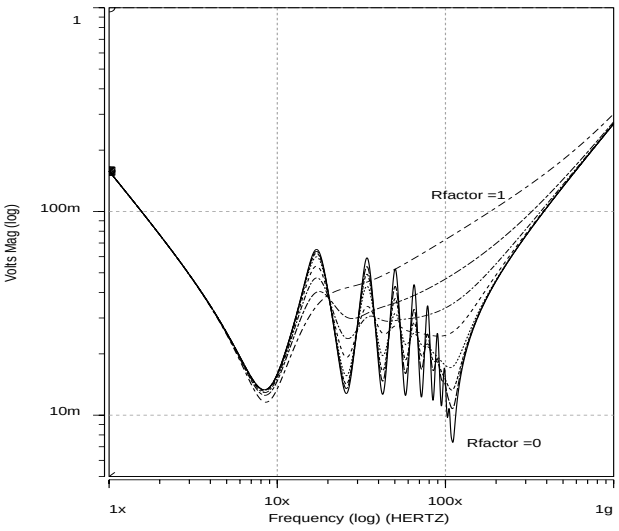

Figure 9: Simulation of transmission line capacitor model with several values of Rfactor. The proportion of loss in the series and parallel positions of the circuit determines the amount of damping.

which is four times longer than the resonator itself. The period of the resonance is $\tau = 1/f_0$. The delay time associated with the quarter wavelength resonator is

$$delay = \frac{\tau}{4} = \frac{1}{4f_0} \quad . \tag{10}$$

This is the delay time from one end of the transmission line capacitor to the other.

The transmission line impedance is $Z_0 = \sqrt{L'/C'}$ and delay for a section is $t'_d = \sqrt{L'C'}$ where L' is inductance, C' is capacitance and the primes indicate per unit length values[10]. From the delay equation, the inductance is $L' = t'^2_d / C'$. The equation is still valid if each parameter is multiplied by length. Even if the length is unknown, the total inductance along the length of the transmission line is equal to the delay time squared divided by the total capacitance $L = t_d^2 / C$. In the case of the MLC capacitor,

$$L_{length} = delay^2 / Cap \tag{11}$$

where L_{length} is the total inductance along the length of the capacitor, *delay* is the time delay from one end of the capacitor to the other and *Cap* is the measured value of capacitance. Substituting equations 10 and 5 into equation 11,

$$L_{length} = \frac{delay^2}{Cap} = \frac{(\frac{1}{4f_0})^2}{Cap} = \frac{(\frac{2\pi\sqrt{ESL \cdot Cap}}{4})^2}{Cap} = (\frac{\pi}{2})^2 ESL \quad . \tag{12}$$

In other words, the inductance along the length of the transmission−line model for the MLC capacitor is $(\pi/2)^2 \times ESL$. For the moment, assume that $L_{cap} \gg L_{mount} + L_{bottom}$. This represents the case where L_{mount} and L_{bottom} have been minimized to insignificance compared to L_{cap}. The total inductance along the length of the transmission−line model is then

$$L_{length} = (\frac{\pi}{2})^2 \times L_{cap} \quad \text{and} \quad L_{sect} = (\frac{\pi}{2})^2 \times \frac{L_{cap}}{n} \quad . \tag{13}$$

Resistance and Loss

After establishing the inductance and capacitance parameters of the transmission−line model, it is necessary to develop the resistance parameters. There are two positions for resistance in the model including the series resistor R_s, which is normally found in transmission−line models, and the parallel resistor R_p. R_p is in series with the capacitive plates but effectively in parallel with the other R_p resistors of the circuit. R_s and R_p have different roles in damping the transmission−line model. It is possible to achieve the correct *ESR* performance (impedance minimum in series resonant circuit) by representing the capacitor loss in either position of the circuit. If all of the capacitor *ESR* is represented by R_p, the value of R_p would be $n \times ESR$. If all of the capacitor *ESR* is represented by Rs, the value for R_s would be $(\pi/2)^2 \times ESR/n$. The $(\pi/2)^2$ factor applies to the series resistance as well as the series inductance. These two scenarios represent the two extremes for representing the loss of the capacitor. It is possible to assign a portion of the loss to R_p and another portion to R_s by using R_{factor}, where R_{factor} is a number between 0 and 1.

$$R_p = ESR \times n \times R_{factor} \qquad R_s = (\frac{\pi}{2})^2 ESR \frac{1 - R_{factor}}{n} \quad . \tag{14}$$

The role of R_{factor} , R_s and R_p is demonstrated through simulation.

Simulation

Figure 9 shows simulated impedance results with R_{factor} taking on several values between 0 an 1 in a geometric progression (0, 0.01, 0.02, 0.04, 0.1, 0.2, 0.4 and 1). One amp has been forced into the terminals of the transmission−line model so the voltage is interpreted as impedance in Ohms. The damping for the transmission line capacitor model is determined by the proportion of *ESR* represented in the R_p and R_s positions of the circuit. For these simulations, L_{mount} and L_{bottom} are zero. At high frequency, the capacitor finally becomes inductive because a "T" representation has been made for the transmission line section. If a "Π" representation, with capacitance nearest the input rather than inductance, had been used the model would have shown capacitive performance at high frequency.

Simulation is used to demonstrate the role of L_{mount} and L_{bottom} . Figure 10 shows simulated impedance results for several values of L_{mount}. R_{factor} is kept constant at 0.7, indicating that 70% of the *ESR* is in the parallel position and 30% of *ESR* is in the series position of the circuit, which is typical for many measured devices. L_{mount} is increased from 10 pH to 4 nH in a geometric progression (10pH, 20pH, 40pH, 100pH, 200pH, 400pH, 1nH, 2nH, 4nH). For very low values of mounting inductance, the transmission line behavior of the capacitor is observed. As the mounting inductance becomes higher the impedance vs frequency curve for the capacitor reverts back to simple RLC behavior. Capacitors must be measured on very low inductance

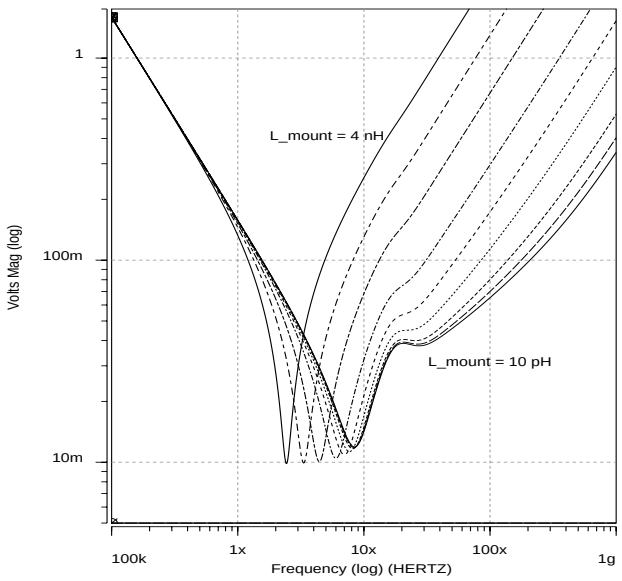

Figure 10: Simulation of circuit model with several values of mounting inductance. Low inductance shows transmission line behavior. High inductance simulation is very similar to simple RLC model simulation.

fixtures in order to observe the transmission line behavior and to measure the parameters for the MLC transmission−line model. If it were possible to completely eliminate $L_{mount}+L_{bottom}$, the transmission line nature of the capacitor would be readily observed.

For CAD simulation, it is desirable to separate out L_{mount} from the capacitor characteristics. L_{mount} is determined by the substrate layout but L_{bottom} and L_{cap} depend upon capacitor design. It is possible to obtain the value of $L_{mount}+L_{bottom}$ from the measurements in Figure 7. A good estimate is simply the inductance given for L_{high} in equation 5. L_{cap} is the difference between ESL and $L_{mount}+L_{bottom}$.

$$L_{cap}=ESL-(L_{mount}+L_{bottom}) \quad . (15)$$

L_{mount} is measured by shorting the fixture by itself and using the same calculation as shown in equation 5.

Model to Hardware Correlation

Figure 11 shows the impedance of two different fixtures with a shorting bar, together with the measurement of a capacitor mounted on the fixtures. The inductance for the wire fixture shown in Figures 4 and 5 has been calculated from equations 1 and 5 and is 83 pH. The second fixture is consistent with PCB geometries and has a higher inductance, 135 pH. The same capacitor has been mounted on each fixture. Also shown in Figure 11 is the simulated results using the transmission−line model and parameters obtained from measurement. Transmission−line model simulation has good agreement with hardware measurements in the capacitive, series resonance (ESR) and inductive portions of the curve. The traditional series RLC model fails to predict the correct inductance and ESR at frequencies above series

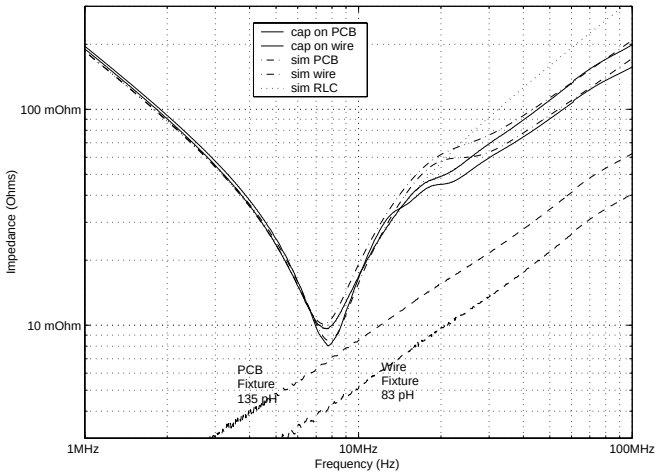

Figure 11: Measured and and simulated transfer impedance results for 1 uF capacitor mounted on wire and PCB (low and medium inductance) fixtures. The fixtures were shorted with a shorting bar to obtain the value of Lmount.

	Wire Fixture	PCB Fixture	Units
Cap	846	846	nF
L_mount	83	135	pH
L_bottom	120	120	pH
L_cap	275	275	pH
ESR	7.9	7.9	mOhms
R_factor	0.9	0.9	
R_mount	1.7	0.0	mOhms

Table 1: Circuit parameters obtained from measurement and used for simulation.

resonance. This is very important for electronic systems performance as demonstrated in [6].

The equations given above are used to calculate the simulation parameters given in table 1. To obtain the best model to hardware correlation, 60 pH has been subtracted from L_{bottom} and added to L_{cap}. This is because some portion of the inductance of the working plates of the capacitor is engaged in the measurement of L_{high}.

Figure 12 shows model to hardware correlation results for several MLC capacitors with several different values, mounted on the low−inductance test fixture. The parameters for each capacitor have been measured as described above. The transmission−line model for capacitors accurately predicts the impedance of measured capacitors in the capacitive, ESR and inductive portion of the curve. Transmission line properties (multiple resonances) can be seen for many of the capacitors.

Accuracy:

A small amount of error is found in the transmission line resonance portion of the curves of Figure 11. To be completely accurate, the model must account for the mutual inductance between each of the partial inductances of Figure 3. Measurement of the mutual inductance is difficult. It may however be possible to extract the self and mutual inductances for the mounted capacitor with electromagnetic extraction software. This is suggested for further work.

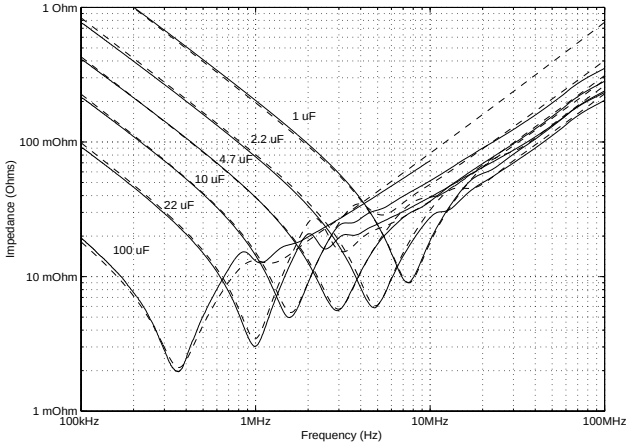

Figure 12: Measured and simulated transfer impedance results for several capacitors.

Accuracy is also related to the number of sections for the distributed transmission−line model. The number of sections is not related to the number of physical plates. There must be sufficient sections in the model to support the number of resonances observed in the measured data. Also, there must be sufficient sections in the model such that $L_{sect}/2$ and $R_s/2$ are insignificant compared to the inductance and resistance of the mounting structure. Ten sections have been sufficient to achieve good model to hardware correlation in this study. The best CAD tool simulation time is achieved with a minimum number of sections.

Conclusion

Transmission−line models for MLC capacitors are desirable for CAD tool simulation of power distribution components. A transmission line topology has been proposed that includes individual inductances for the mounting structure and the filler plate inside the physical capacitor. Measurement techniques that obtain each of the circuit model parameters have been demonstrated. Simulation results for the transmission−line model closely match the measured transfer impedance for MLC capacitors mount on low inductance fixtures.

Acknowledgments

The authors would like to thank Ray Anderson for his expertise with digital photographs.

References

[1] S. Daijavad and H. Heeb, "On the effectiveness of decoupling capacitors in reducing EM radiation from PCBs," Symposium Record, 1993 IEEE International Symposium on Electromagnetic Compatibility, pp. 330−333, August 1993.

[2] T. Roy and L. Smith, "Power plane decoupling strategy for high−speed processor boards," Conference Record, Electrical Performance of Electronic Packaging, San Diego, CA, pp. 141−144, October 1999.

[3] Power Integrity Module of SpecctraQuest CAD Tool, Cadence Design Systems, www.cadence.com.

[4] K. Chen, W. Brown, L. Shaper, S. Ang, and H. Naseem, "A study of the high−frequency performance of thin film capacitors for electronic packaging," IEEE Transactions on Advanced Packaging, vol. 23, pp. 293−302, May 2000.

[5] Y.−L. Li, M. Elzinga, and F. Yahyaei−moayyed, "Distributred models for multi−terminal capacitors−using 2D lossy transmission−line approach," Proceedings of 2001 Electronic Components and Technology Conference, 2001.

[6] L.D.Smith, D.Hockanson, "Distributed SPICE Circuit Model for Ceramic Capacitors," *Proc 51st Electronic Components & Technology Conference*, Lake Buena Vista, FL, May.2001, pp. 523−528.

[7] G. Hjellen, "Including dielectric loss in printed−circuit models for improved EMI/EMC predictions," IEEE Transactions on Electromagnetic Compatibility, vol. 39, pp. 236−246, August 1997.

[8] A. Scarlatti and C. Holloway, "An equivalent transmission−line model containing dispersion for high−speed digital lines− with an FDTD implementation," IEEE Transactions on Electromagnetic Compatibility, vol. 43, pp. 504−514, November 2001.

[9] David M.Pozar, Microwave Engineering, Addison−Wesley, (1990), p 236.

[10] John D. Kraus, Electromagnetics, Fourth Edition, McGraw−Hill, (1992), Chapter 12.