Published in Conference Record, Electrical Components Technology Conference (ECTC), Lake Buena Vista, Florida, pp. 523-528, May 29, 2001.

Distributed SPICE Circuit Model for Ceramic Capacitors

Larry D Smith, David Hockanson
Sun Microsystems, Inc. MS MPK15-103
901 San Antonio Road, Palo Alto, CA, 94303-4900
Phone: 650-786-3303, FAX: 650-786-6457
larry.smith@sun.com, david.hockanson@sun.com

Abstract

Discrete ceramic capacitors are used to achieve a low power supply impedance in the MHz range. The traditional series RLC circuit model for discrete capacitors is inadequate for low ESR capacitors when mounted on low ESL pads. When combined with other capacitors or power plane models, the simple RLC model does not correctly predict the magnitude or frequency of the anti-resonant peak formed by the parallel components. Discrete capacitors have higher ESR and lower inductance than expected at frequencies above series resonance. A new distributed circuit model is proposed for high Q, low ESR capacitors. The distributed model correlates well with hardware measurements. Both simulated and measured results indicate that anti-resonant peaks are higher in frequency and lower in magnitude than predicted by the traditional series RLC model. Low ESR capacitors do not create the high impedance peak expected from simulation of the traditional series RLC circuit model.

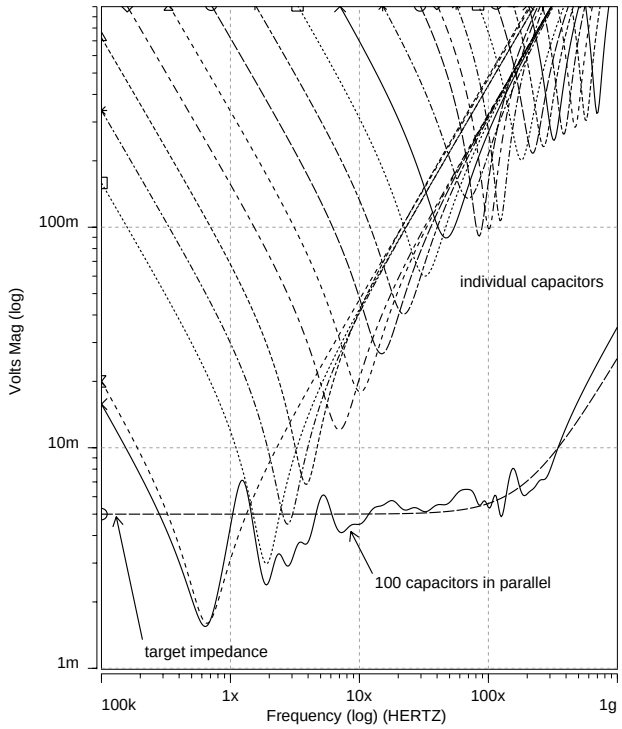

Figure 1: Several values of capacitors are placed in parallel to meet the target impedance for a product. The impedance profiles are the results of SPICE simulation with a traditional RLC capacitor model.

Introduction

Computer systems continue to demand higher power at lower voltage. It is a significant challenge to design a power-distribution system that is capable of delivering large amounts of current at low voltage. Silicon chips require a tight voltage tolerance (i.e. 5%) in order to perform properly. Therefore a next generation product requires an ever decreasing power supply impedance. The clock frequency of microprocessors continues to rise, therefore a low impedance power supply is necessary for an increasing frequency range.

The primary components of the power distribution system include the voltage regulator module, discrete decoupling capacitors and printed circuit board (PCB) power planes. Advanced computer systems may be crowded with hundreds of small ceramic capacitors, which are the means for providing a low-impedance path for power in the MHz range. Capacitors must be chosen and placed to optimize performance with smaller quantities given the component density of PCB's as well as occasional supply issues. A new model for discrete ceramic capacitors mounted on PCB power planes is presented in this paper. The model is appropriate for SPICE simulation and for analysis programs that optimize the use of discrete capacitors.

One method of optimizing capacitor selection and location for product performance involves the identification of a target impedance and selection of capacitors to meet that target impedance over a broad frequency range [1]. The target impedance for a product is calculated as

$$Z_{target} = \frac{Vdd \times ripple}{trans\ current} = \frac{2.0V \times 5\%}{20\ amp} = 5\ mOhm$$

In this example, a product with a 2 volt power supply may abruptly draw a 20 amp transient current. A power distribution system (PDS) with an impedance of 5 mOhms or less will result in an acceptable amount of regulation noise. The PDS must meet the target impedance up to a frequency associated with the rise time of the transient current. The simulation results in Figure 1 shows how several different values of capacitance may be placed in parallel to meet a target impedance over a broad frequency range. One hundred capacitors have been placed in parallel to meet the 5 mOhm target impedance from 1 to 200 MHz.

Traditional Series RLC SPICE Model

Ceramic capacitors have traditionally been modeled as a series RLC network. Capacitor vendors usually describe the specifications for a capacitor in terms of it's capacitance, equivalent series resistance (ESR) and equivalent series inductance (ESL). These parameters work well for moderately high ESR capacitors with a moderately low Q, and when capacitors are mounted on pads that dominate the ESL. A series RLC circuit model has been assumed for each of the capacitor's simulated in Figure 1.

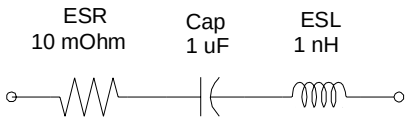

Figure 2: Traditional RLC circuit model for capacitor.

The traditional RLC series circuit is shown in Figure 2. Figure 3 shows the impedance versus frequency of this circuit. The RLC components are constant with frequency and are easily identified on the Bode plot. The capacitive portion has a slope of -20 dB/decade and the inductive portion has a slope of +20 dB/decade. The curve bottoms out at an impedance equivalent to the ESR value at the series resonant-frequency. The minimum is at the frequency

$$f_{min} = \frac{1}{2\pi\sqrt{ESL \cdot Cap}} = \frac{1}{2\pi\sqrt{1nH \cdot 1uF}} = 5M$$ (Eqn 1),

where f_{min} is the frequency of the low impedance dip associated with series resonance.

Q or quality factor for an RLC circuit is equivalent to the reactive impedance divided by the resistance.

$$Q = \frac{Z}{R} = \frac{\sqrt{ESL/Cap}}{ESR} = \frac{2\pi \cdot f_{min} \cdot ESL}{ESR} = \frac{\omega}{}$$

Q is an indication of the sharpness of the resonance. The Q of the circuit is reduced by reducing L. The ratio of L/R is important. With a reduction in L, ESR can be reduced without increasing the Q of the circuit. High Q capacitors can lead to high impedance anti-resonant peaks if not managed properly.

Capacitors on PCB Power Planes

For advanced computer systems, capacitors are typically surface mounted on a PCB and connected directly to Vdd and Gnd power planes with vias. This section describes how the characteristics of power planes and capacitors mounted on power planes are measured and simulated. The traditional RLC model for the capacitor is shown to be inadequate because it does not correctly predict the parallel anti-resonance with the power planes.

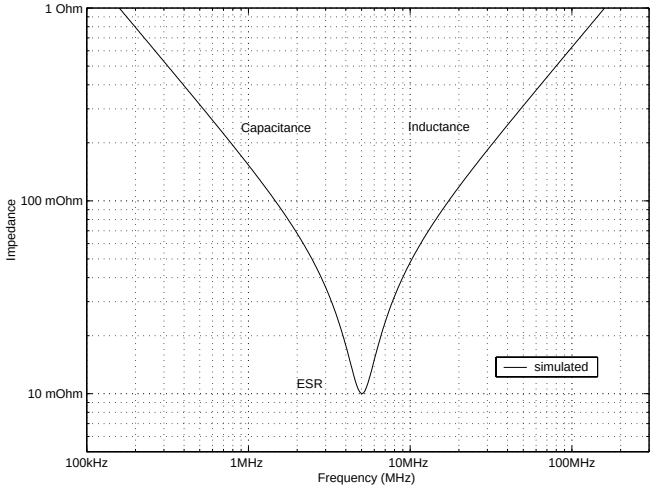

Figure 3: Impedance versus frequency for traditional RLC capacitor model.

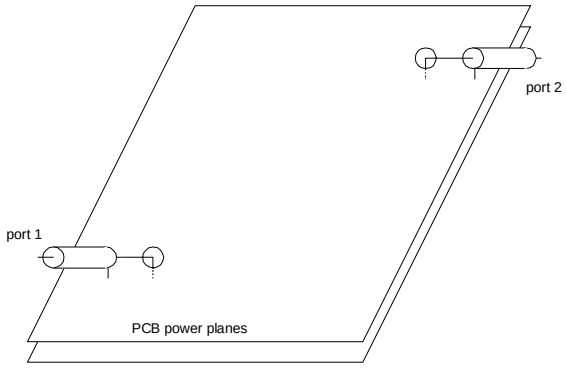

Figure 4: Measurement of PCB power planes with VNA.

PCB power planes are two parallel plates of conducting material which form a parallel plate capacitor at low frequencies. At higher frequencies, they develop impedance resonances that are associated with their parallel plate geometry [2].

The power plane transfer impedance (transimpedance) is measured as shown in Figure 4 and described in [3]. A vector network analyzer (VNA) is used to make an S21 measurement. The instrument is calibrated by connecting the 50 Ohm transmission lines associated with Port 1 and Port 2 together and doing a "through" calibration which is set as the reference level of 0 dB. The transmission lines are then soldered to vias connected to the PCB power planes. Power is injected into Port 1 and power delivered is measured at Port 2. The transimpedance of the power planes is calculated from the magnitude of S21 (in dB) from

$$|S_{21}| = 20\log_{10}\frac{|Z_{plane}|}{25\,ohms} \text{ and } |Z_{plane}| = 25 \cdot 10^{\frac{|S_{21}|}{20}}.$$

A SPICE model has been developed that correctly simulates the capacitance at low frequency and the cavity resonances at higher frequencies [4]. SPICE simulation is done by injecting 1 AC amp into the power planes at one position, measuring the voltage at another position and dividing voltage by current to get transimpedance. Figure 5 shows the measured and simulated impedances for a pair of 4.1 x 9.5 square inch power planes spaced 3 mils apart. The dielectric was FR4 and was assumed to have a dielectric

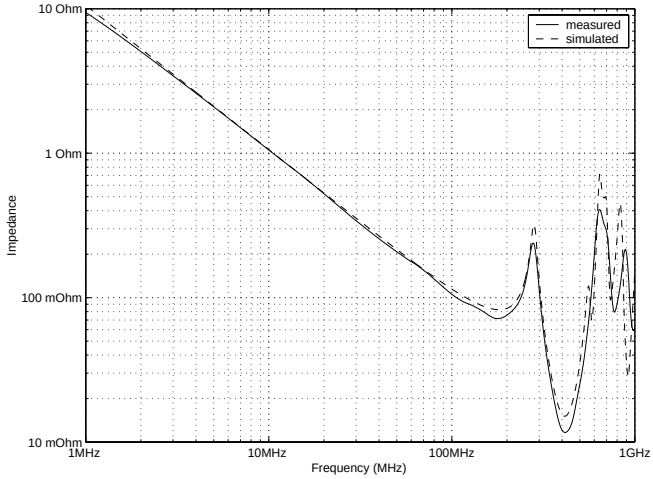

Figure 5: Measured and simulated impedance versus frequency for PCB power planes.

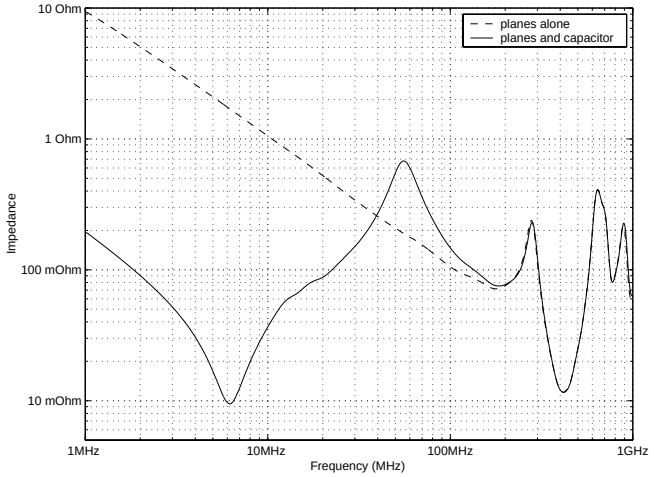

Figure 6: Measured Power planes impedance,with and without 1 uF capacitor.

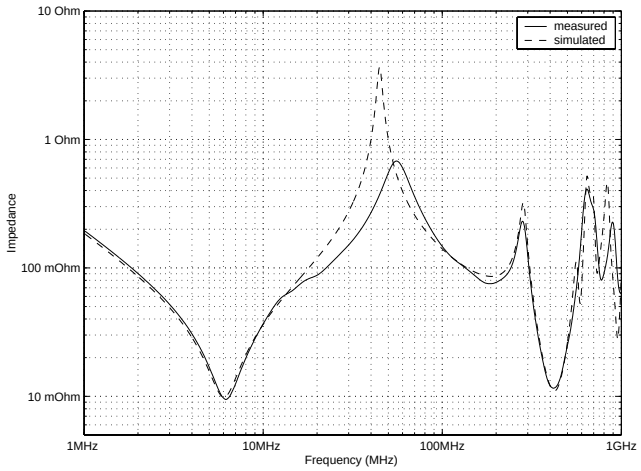

Figure 7: Measured and simulated impedance of capacitor on power planes. Traditional RLC model gives incorrect anti-resonant peak.

constant of 5.05. Model to hardware correlation for the power planes is good. At low frequency, the power planes are capacitive. Cavity resonances that develop above 100 MHz are correctly predicted by the model.

A single 0603 size, X5R dielectric, 1 μF capacitor is soldered to PCB pads with vias connected to the same power planes. Simulation and measurement is performed by the same method. Figure 6 shows the measured response of the power planes with and without the capacitor. The capacitor causes a low impedance series resonance at about 6 MHz. It also causes an impedance peak at about 50 MHz. This is the parallel anti-resonance of the capacitor with the power planes [5]. The capacitor has become an inductance above it's series resonant frequency. It is in parallel with the capacitance of the power planes and forms the classic LC tank circuit with an impedance peak.

The circuit parameters for the capacitor and power planes are calculated from the measured impedance and frequency. Capacitance is calculated by finding the impedance at a point on the down sloping curve and using the relationship

$$Z = \frac{1}{j\omega C} \quad \text{and} \quad C = \frac{1}{2\pi \ frequency|Z} \ .$$

Capacitor ESR is found from the impedance at series resonance. Capacitor ESL is found from Equation 1. Table 1 summarizes the parameter calculations. The capacitor was measured to be 0.820 uF with 9.5 mOhm ESR and has 815 pH of inductance when mounted on the PCB.

The measured capacitor parameters are used in SPICE simulation of the traditional RLC model mounted at the proper position on the power planes. The simulated and measured results are shown in figure 7. Good model to hardware correlation is obtained at all frequencies except for the parallel anti-resonant frequency. Both the frequency and the magnitude of the simulated peak are incorrect. The frequency of the peak is associated with the ESL and the height of the peak is associated with the ESR. Both parameters are a function of frequency. The frequency of the measured peak is

$$f_{peak} = \frac{1}{2\pi \sqrt{ESL \frac{Cap \cdot C_{plane}}{Cap + C_{plane}}}} \quad \text{and,}$$

$$ESL = \frac{1}{\left(2\pi \cdot f_{peak}\right)^2 C_{plane}} = \frac{1}{\left(2\pi \ 55.4MHz\right)^2 \frac{820nF \cdot 15nF}{820nF + 15nF}} \ .$$

The inductance of the mounted capacitor is apparently 815-560=255 pH less at the parallel anti-resonance than it is at the series resonant frequency. The traditional series RLC model does not predict the correct anti-resonant peak when the capacitor is mounted on power planes in a common decoupling application because ESR and ESL are functions of frequency.

structure	dB1	freq 1 (MHz)	dB2	freq 2 (MHz)	C (nF)	ESR (mOHms)	ESL (pH)
power planes	-28.57	11.31			15		
1 uF capacitor	-42.20	1.00	-68.43	6.16	820	9.5	815

Table 1: Measured values for power planes and a mounted capacitor using S21 parameters.

Distributed Circuit Model for Discrete Capacitor

A clue for a more accurate circuit model comes from the physical construction of the capacitor. Figure 8 shows a cross section of a discrete capacitor mounted on a PCB with Vdd and Gnd power planes. Current travels around a loop that includes the vias, decoupling capacitor pads and the capacitor itself. The capacitor consists of two vertical posts attached to many interleaving plates in between.

The power planes on a well designed PDS may be separated by 2 mils and may be just 6 mils from the surface of the PCB. In contrast, the capacitor height may be 40 mils or more. The current path around the loop starts on the Vdd plane and continues up through a via and solder pad to the capacitor post. From here, it either continues up the post or heads out laterally on one of the plates. Current always follows the path of least impedance and distributes itself accordingly. Eventually, all current paths lead to capacitor plates where conduction current becomes a displacement current through the ceramic dielectric. The current path completes the loop through the right post, pad and via structure of the PCB, and finally to the Gnd power plane.

Figure 9 shows a circuit model for SPICE simulation that duplicates the construction of the capacitor mounted on the PCB. There is a ladder structure with capacitive and resistive plates forming the rungs on the ladder. Each plate is

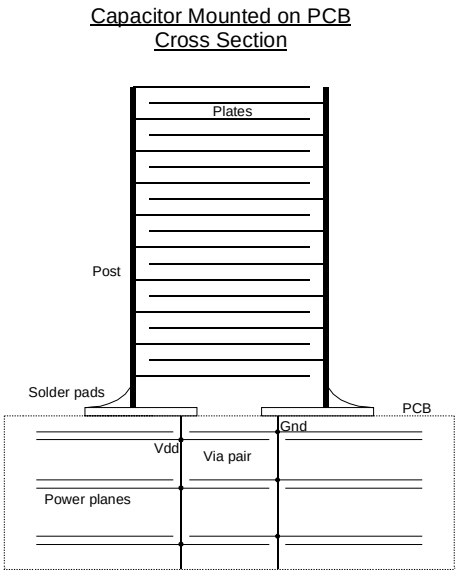

Figure 8: Cross section of discrete capacitor mounted on PCB power planes.

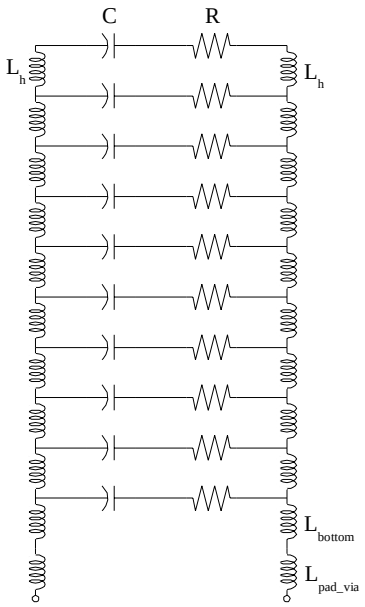

Figure 9: Distributed circuit model for SPICE derived from construction of ceramic capacitor.

composed of thin metal with a resistivity. Resistance of the plates is responsible for most of the capacitor's ESR. Dielectric loss contributes very little to the lossyness of a ceramic capacitor below 1 GHz. A portion of the ESR is therefore associated with each distributed capacitor plate.

Inductance is always associated with a loop of current. With a larger loop, more magnetic flux is stored in the environment creating a larger inductance. Current that travels across the bottom plates and then back to the power planes makes a smaller loop than current that goes all the way to the top of the capacitor. Therefore, the vertical standards of the ladder model are inductors. Current that goes to the top of the ladder must go through more inductance than current that goes across the bottom of the ladder.

Parameters for the components of the distributed model are determined empirically. By the shorting bar resonance method [6] [7], the loop inductance of the via and pads in the PCB are found to be 350 pH. The distributed model therefore has 350/2 = 175 pH of inductance on each side at the base of the ladder. There is some inductance associated with the solder connection between the PCB pads and the capacitor posts. There is more inductance associated with the physical distance inside the capacitor from the bottom of the post to the first plates. One hundred and fifty pH loop inductance has been attributed to this vertical height, 75 pH per sided. The rest of the inductance of the capacitor is associated with the loop in which current travels as it flows up the posts and across the plates of the capacitor, and back down again.

Reasonable values for the vertical inductances are found after making the simplifying assumption that at series resonant frequency, all plates of the capacitor are equally engaged with current. The total ESL of the mounted capacitor is found from Equation 1 is 815 pF. A portion of that ESL is in the power planes, vias, solder pads and distance to the first plates (350+150=500pH). The remainder of the ESL is in the capacitor height and distributed throughout the rest of the ladder. The internal inductance for the 1 uF capacitor with this topology is:

$$L_{height} = ESL_{meas} - L_{mount} = 815 - 500 = 315\ pH \ .$$

For the circuit topology of Figure 9, there are 10 horizontal rungs for the distributed ladder model. The capacitance, resistance and inductance parameters need to be adjusted according to n, the number of parallel paths in the circuit topology.

$$C = \frac{cap}{n} \qquad R = ESR \cdot n \qquad L_h = \frac{2.5 L_{heig}}{2n} \ .$$

The capacitance and resistance scale as expected when the parameters are distributed into the ladder network. But there is 2.5 times the inductance that might have been expected. This achieves the best model to hardware correlation at series resonance. L_{bottom} is optimized to obtain the frequency and height of the parallel anti-resonance. The parameters calculated above for n=10 are summarized in table 2.

Element	Value	Calculation
L_pad_via	175 pH	Measured
L_bottom	75 pH	Best fit
L_h	34.9 pH	2.5*[ESL – (L_pad_via + L_bottom)]/2n
C	82.0 pF	capacitance/n
R	95 mOhm	ESR*n

Table 2: Element values for Figure 9 used in model to hardware correlation.

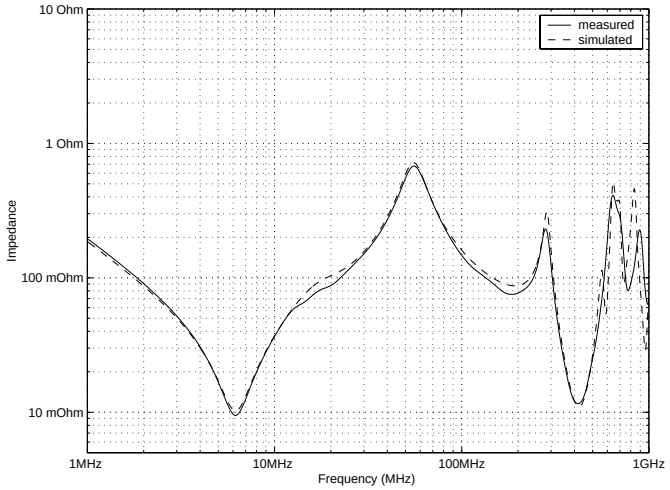

Figure 10: Distributed circuit model simulation compared to measured 1 uF capacitor mounted on power planes. Good model to hardware correlation.

Figure 10 shows the distributed capacitor model simulation compared to the measured impedance. The anti-resonant peak matches much better than it did with the traditional RLC model. The frequency dependent ESR and ESL have been properly accounted for.

Internal Capacitor Currents

The current distributes itself within the circuit model according to the path of least impedance. The reactance of an inductor is jωL and is proportional to frequency. The reactance of a capacitor is 1/(jωC) and is inversely proportional to frequency. At low frequencies, the inductance represents a small reactance (impedance) and the capacitors are a large reactance. Current distributes itself equally on all plates of the capacitor because the current is capacitance limited. But at higher frequency, the inductor impedances increase and the capacitor impedances decrease. Current is discouraged from going high up the ladder because of increased impedance.

Figure 11 shows the internal currents for the simulated capacitor. All of the injected 1 amp flows through the bottom inductor. At low frequency, an equal portion of the amp flows through each capacitor. Figure 11b shows the current diminishing in each sequential inductor of the ladder. Figure 11c shows that each of the 10 capacitors carries 1/10 of the current at low frequency. This validates the assumption that at series resonant frequency (dip) all plates are equally engaged.

At the parallel resonant frequency, there is a peak of current in both the inductors and the capacitors. There is nearly 4 amps entering the bottom of the capacitor, even though only 1 amp was forced into the PCB. This is because charge is resonating back and forth between the PCB capacitance and the discrete capacitor. As frequency increases, a higher percentage of the current stays down low in the capacitor as the vertical inductances become higher in impedance. This forces the current to to go through higher resistance because only the lower plates of the capacitor are engaged. As frequency goes up, the ESL of the capacitor is reduced and the ESR of the capacitor is increased.

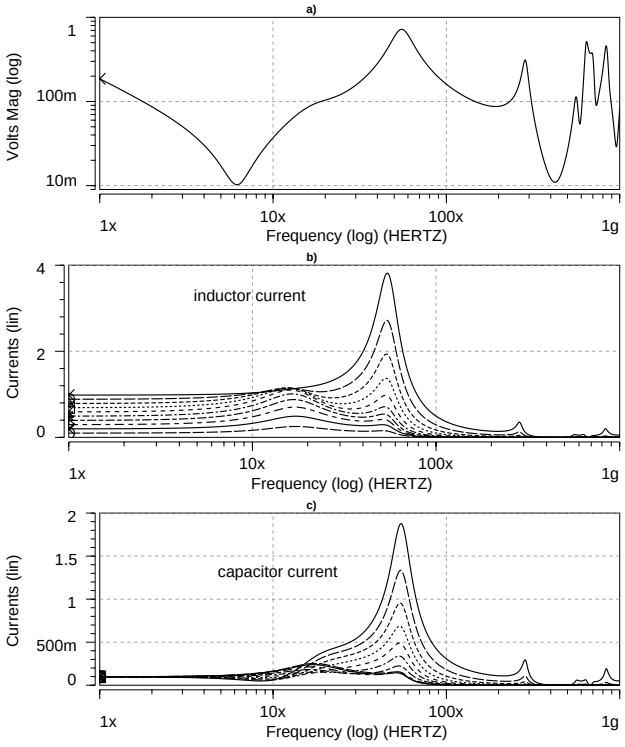

Figure 11: SPICE simulation of internal currents for the distributed capacitor. a) Board impedance with 1 uF capacitor. b) Inductor currents. c) Capacitor currents.

Low ESR Capacitors for Decoupling Applications

Some product designers have been reluctant to use low ESR capacitors in decoupling applications because of the anti-resonance issue. High Q capacitors can form a high impedance parallel anti-resonance with another discrete capacitor or with the capacitance of the power planes. However, measured results reveal that the anti-resonance is not as high as expected from analysis with a simple RLC circuit. As frequency goes up, the ESR is higher and the inductance is lower than expected, both of which reduce the Q of the circuit and reduce the height of the parallel anti-resonance. The anti-resonance from high Q capacitors is not a serious problem when capacitors are mounted on low inductance pads. A further reduction of the mounting inductance lowers the Q even more and further reduces the height of the anti-resonant peak.

There is much to be gained from low ESR capacitors in a methodology such as described in [1] and illustrated in Figure 1. Low ESR capacitors are able to achieve a specified target impedance more efficiently than high ESR capacitors. When managed properly, capacitors with a Q between 2 and 5 work very nicely. For capacitors with a series resonance more than 100MHz, even higher Q is desirable. Low ESR capacitors are very beneficial when used in this way and do not create high impedance anti-resonant peaks as might have been expected.

Conclusions

The traditional series RLC circuit model for a discrete capacitor is inadequate. It predicts a much higher parallel anti-resonant peak when the capacitor is simulated with another high frequency capacitor or on PCB power planes than is actually measured in hardware. The ESR and ESL of a mounted discrete capacitor is a function of frequency. As frequency goes up, the inductance associated with the height of the capacitor causes current to stay down low in the capacitor. Fewer plates carry most of the current leading to higher ESR. The current stays closer to the return current in PCB power planes leading to lower inductance. The Q of capacitors is reduced at high frequency by this effect, and the anti-resonant peak is reduced. A distributed circuit SPICE model captures this effect and correlates well with hardware measurements. Low ESR capacitors are very useful for decoupling applications. The anti-resonant peak associated with high Q capacitors is easily managed.

References

1. L.D.Smith, R.E.Anderson, D.W.Forehand, T.J.Pelc, T.Roy, "Power Distribution System Design Methodology and Capacitor Selection for Modern CMOS Technology," IEEE Transactions on Advanced Packaging, Vol.22, No.3, August 1999, P284.
2. S.Pannala, J.Bandyopadhyay, M.Swaminathan, "Contribution of Resonance to Ground bounce in Lossy Thin Film Planes," IEEE Transactions on Advance Packaging, Vol.22, No.3, Aug 1999, P249.
3. I.Novak, Measuring Milliohms and PicoHenrys in Power Distribution Networks," Design Con 2000.
4. L.D.Smith, T.Roy, R.E.Anderson, "Power Plane SPICE Models for Frequency and Time Domains," Proc. EPEP Conference, Oct.2000
5. T.Harada, H.Sasaki, Y.Kami "Controlling Power-Distribution-Plane Resonance in Multilayer Printed Circuit Boards." IEICE Transactions. Commun., Vol.E83-B, No.3, March 2000.
6. T.Hubing, J.Drewniak, T.Van Doren, D.Hockanson, "Power Bus Decoupling on Multilayer printed Circuit Boards," IEEE Transactions on Electromagnetic Compatibility, Vol. 37, No. 2, p155, May 1995.
7. L.D.Smith, T.Roy, R.E.Anderson, "Power Plane SPICE Models for Frequency and Time Domains," IEEE Transactions on Advanced Packaging, to be published.