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Power Plane SPICE Models and Simulated Performance for Materials and Geometries

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Abstract

A SPICE model for power plane simulation has been developed. It is based on the geometries and materials of the power planes and uses a unit cell composed of RLC elements, transmission line elements or the HSPICE W-element. Simulated resonances in the frequency domain and delays in the time domain are consistent with results calculated from physical dimensions. Spice model simulations compare well with hardware measurements in both the frequency and time domains. The role of dielectric thickness, dielectric constant and parallel pairs of power planes is demonstrated through simulation. Spreading inductance of power planes is defined, discussed and measured. Power plane performance in terms of impedance, resonances, damping and spreading inductance is optimized by the use of a thin dielectric layer between conductive planes.

I. Introduction

Power planes are used to deliver power to both core logic and I/O circuits in modern computer systems. With each computer generation, the amount of power required is ever increasing. As silicon technology advances, scaling has required that the power supply voltage be reduced. Therefore the current delivery requirements for the power planes has gone up greatly and the tolerance for noise has gone down. The power delivery system is required to be low impedance from DC to high frequency, possibly several GHz [1]. The power planes are capacitive at low frequencies, then develop resonances according to their cavity dimensions [2],[3],[4] at high frequencpaper2.sdwies.

This paper will examine the characteristics of power planes in delivering low impedance power at high frequency. It is divided into four major sections. In section II, a method of modeling the power planes in SPICE is given. Three different unit cells are proposed and the merits of each are discussed. The accuracy of the SPICE model is verified by comparing it to known physical results and to hardware measurements in section III. The SPICE model is used to examine important power plane properties that are a function of the materials and geometries in section IV and used to evaluate spreading inductance in section V. Conclusions are drawn about the best materials and geometries for achieving power planes with low impedance and low spreading inductance leading to optimal noise performance.

II. Power Plane Spice Models

Power Planes have been modeled as an array of SPICE circuit elements in [5] and [6] using frequency independent parameters. In order to account for the frequency dependent resistance from skin effect, power plane characteristics were extracted in MDS and the n-port s-parameters were simulated in SSPICE. In the present paper, a similar approach is used to obtain capacitance and DC resistance. However, inductance is obtained from wave velocity considerations rather than the product of permeability and dielectric thickness. This has advantages when perforated planes are considered. The frequency dependent parameters that account for skin effect and dielectric loss are accounted for by frequency dependent resistors or the Avanti Star HSPICE W-element transmission line model [7], [8]. In the previous work, unit cells that represent a pre-defined surface area were connected together to form the length and width (or irregular shape) dimensions of the power planes. In the present method, a fixed topology is used (e.g. 8x8 array of orthogonal transmission lines). One advantage of this method is that all calculations for power plane parameters can be made within the HSPICE execution. S parameters are not imported. The inputs to the HSPICE program include the power plane length, width, dielectric constant and thickness, and conductor conductivity and thickness. Another advantage is that all rectangular shaped power planes may be simulated without changing the unit cell or array topology.

The parameters of the circuit elements are based on simple calculations that relate directly to the materials and geometries used to construct the power planes [9] and are briefly reviewed here. The capacitance per unit area is

$$C_a = \frac{\epsilon}{thickness} \quad \text{(farads/cm}^2\text{)} \qquad (1)$$

where where $\varepsilon=\varepsilon_0\ \varepsilon_R$ is the electrical permittivity. The velocity of a plane wave traveling between the parallel plates of the power planes is calculated from the dielectric reduced speed of light.

$$velocity = \frac{c_{light}}{\sqrt{\epsilon_R}} \quad \text{(cm/sec)} \qquad (2)$$

where ε_R is the relative permittivity of the dielectric and c_{light} is the velocity of light in free space. The velocity of propagation on a transmission line is $1/\sqrt{LC}$ where L and C are the inductance and capacitance per unit length. A similar calculation is made for velocity on power planes using spreading inductance and capacitance per area C_a. Spreading inductance L_a is defined from

$$velocity = \frac{1}{\sqrt{L_a\ C_a}} \quad . \quad L_a = \frac{1}{\left(C_a\ velocity^2\right)} \frac{henries}{square} \qquad (3)$$

Spreading Inductance (similar to spreading resistance) is calculated from C_a and velocity and has units of henries per square. From inductance and capacitance, impedance and delay for power planes are calculated.

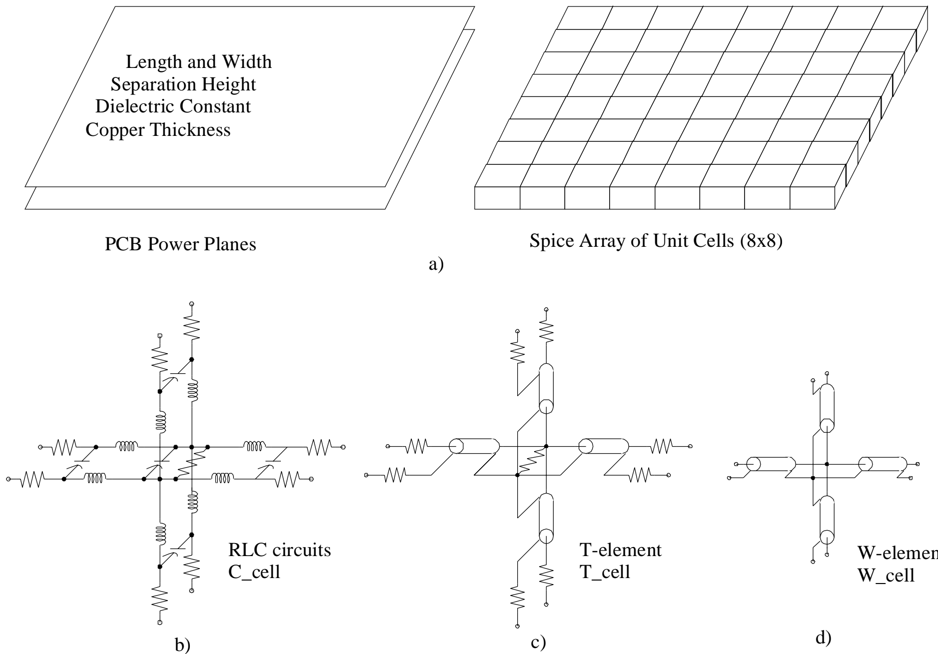

Figure 1: a) PCB power planes have geometric and material properties. They are divided into unit cells. Three different unit cells are analyzed: b) C_cell, c) T_cell and d) W_cell.

$$Z_{p0} = \sqrt{L_a / C_a} \quad \text{(ohm-cm)} \tag{4}$$

$$t_{delay} = \sqrt{L_a\, C_a} \quad \text{(sec/cm)} \tag{5}$$

Z_{p0} is the impedance to a plane wave traveling in a width of the power plane material. The interpretation of power plane impedance in ohm-cm is that a long strip of power plane material 1 cm wide has an impedance of Z_{p0}. Of the four parameters: capacitance, velocity, inductance and impedance, only two are independent. Any two may be used to calculate the other two. Delay is the reciprocal of velocity.

Loss on power planes is attributed to both conductor and dielectric loss. DC conductor resistance is independent of frequency but skin effect resistance goes as $\sqrt{frequency}$. The thickness of the conductor carrying the current is the minimum of either the thickness of the conductor itself or the skin depth, which ever is the least. After the onset of skin effect, an ever diminishing surface depth carries current as frequency increases. The resistance of a power plane conductor is:

$$R = resistivity * squares = \frac{1}{\sigma \, min(thickness, \delta)} \cdot \frac{length}{width} \tag{6}$$

where $\delta = 1/\sqrt{\mu \pi \sigma \, frequency}$, σ = conductivity of the conductor and μ = permeability of the conductor. Dielectric loss is due to the conductivity of the dielectric which is proportional to frequency and capacitance

$$G = \omega \, C \tan \delta \tag{7}$$

where $\tan \delta$ is the loss tangent of the material, assumed to be constant with frequency.

Model Topology

The parameters calculated above are used in a circuit model to simulate power planes in SPICE. The physical features of the power planes are shown in figure 1a. The plane is divided into an n x n array of unit cells. Three different types of unit cells are given in figure 1b, c&d which involve lumped circuit elements , the SPICE T-element and the HSPICE W-element (T_cell, C_cell, W_cell respectively). Because there are transmission line elements in both the x and y direction, there is a tendency to double count the capacitance of the power planes. Also, the x transmission lines load down the y transmission lines and slow down the velocity. To correct for this, the impedance is increased and the time of flight is decreased by a factor of $\sqrt{(2)}$ for each transmission line element. This causes the total capacitance of the power planes and the time delay across the power planes to simulate correctly with the given topology.

All three unit cells correctly account for frequency dependent loss in the frequency domain. The resistors in the C_cell and T_cell are dependent upon frequency as described above. The W_cell uses the W element which correctly accounts for frequency dependent loss in both the frequency and time domains. The resistors in the C_cell and T_cell do not have a frequency dependence in the time domain and only DC loss is modeled. The C_cell and T_cell will not exhibit the rise time degradation that is a result of frequency dependent loss in the time domain.

The SPICE reference node (zero) is not found in the unit cells or anywhere in the topology of the SPICE power plane models. The unit cells are balanced with respect to the reference node. This becomes important when multiple pairs of power planes are connected in parallel. It is possible to stack several power planes with different voltages on top of each other (e.g. 3V, 5V, Vss and 1.5V, in that order) by simply connecting the nodes of a lower pair of planes to the nodes of an upper pair of planes. All voltages must be measured differentially (vertically) within the stackup. Voltages with respect to SPICE node zero have no physical meaning.

The best place for SPICE node zero is at the negative terminal of the voltage regulator module or off to the side somewhere. It is best if there is one singular reference node in the simulated system. This prevents sneak current paths from occurring. All of the current that enters through the power planes must also exit by the power planes. For every current to the left, there must be a current to the right. All currents must flow in a complete loop. Charge is conserved with this type of model.

Unit Cell Granularity

The granularity (number of unit cells) of the model has implications on run time and accuracy. A dense array of unit cells will give a more accurate solution but will have a higher cost in terms of CPU run time. The most efficient granularity for simulation speed and accuracy is found by considering the frequency content of a rising or falling edge and the maximum length of transmission line that can be used without proper termination.

Transmission lines exhibit resonant phenomenon when they are not properly terminated in their characteristic impedance which leads to incorrect simulation results. The array of transmission lines are inherently miss-terminated at each node because one transmission line is feeding the parallel combination of 3 similar transmission lines. To prevent the miss-termination from becoming a problem, the maximum length of a transmission line segment should be no more than 1/5 of a rise time for a transient waveform. This enables the near end of each transmission line to influence the far end twice during the rise time, thus making reflection errors insignificant. If the transmission line delay between two nodes is τ the minimum rise time is $5\,\tau$.

Most of the frequency content of a waveform is less than $0.35/t_{Rise}$. For good accuracy, the maximum frequency allowed on the power planes with a transmission line segment delay of τ is

$$f_{max} = 0.35/t_{rise} = 0.35/(5\tau) = 1/(14.3\tau) \quad . \quad (8)$$

The period for f_{max} is $1/f_{max} = 14.3\tau$. In other words, a transmission line grid segment should be no more than about 1/15 of the wavelength of the maximum frequency of interest in the SPICE analysis, otherwise reflection errors may occur.

CPU Run Times

The CPU run times for frequency and time domain simulations using the three base cells are compared in table 1. The run times in the frequency domain depend upon the frequency span and the number of points per decade and the run times in time domain depend upon the time span and step size. These parameters were held constant for the three runs involving the three cells, so the relative times can be compared. All three unit cells give accurate results in the frequency domain but only the W-element gives correct frequency dependent results in the time domain. There is a substantial CPU time penalty for this accuracy.

Cell	.ac time	.tr time	Total Time	Units
C	18	3	21	seconds
T	21	5	26	seconds
W	84	29	113	seconds

Table 1: CPU run times for three base unit cells.

III. Demonstration of HSPICE Model Accuracy

In this section, the accuracy and usage of the HSPICE models for power planes is demonstrated. Much physical insight is obtained by examining a power plane that is stimulated along an edge. The simulated results of the unit cell arrays are compared to known characteristics of a capacitor at low frequency and to an open circuited transmission line at higher frequencies where one dimensional resonances are apparent. Then, in a more realistic case, the power planes are stimulated from a single point and compared with hardware measurements.

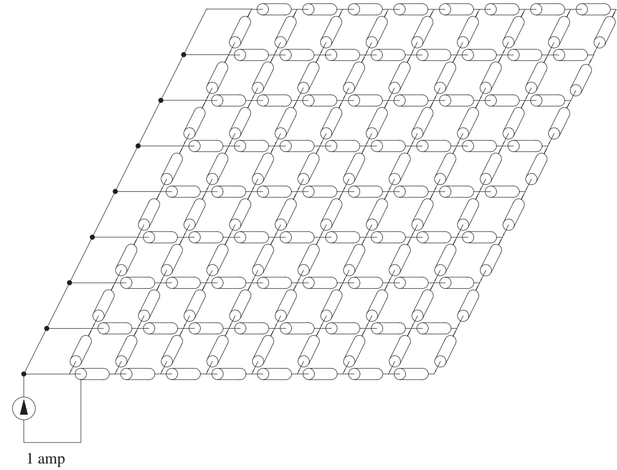

Figure 2: The left hand side of the power planes is stimulated with a 1 amp ac source.

Plane Waves on Power Planes

Consider a pair of power planes that are 6 inches (15.24 cm) square and separated by an $\varepsilon_R = 4$ dielectric. One side of the plane pair is stimulated by connecting the eight Vdd nodes together, connecting the eight Vss nodes together and forcing 1 amp between the planes as shown in figure 2. The frequency domain voltage measured vertically between any two vertical points on the stimulated edge is the impedance.

Results are shown for the frequency domain in figure 3a. At low frequencies, the power planes behave like a parallel plate capacitance. The capacitance is

$$C_a \cdot area = \frac{\epsilon_R \epsilon_0}{thickness} length\, width = 8.1nF \quad (9)$$

The known impedance of 8.1 nF at 10 MHz is $Z = 1/j\omega C = 1.96\, ohms$. The simulated impedance of the power planes at 10.2 MHz is 1.98 Ohms, very close to the expected value.

The time delay across the 6 inch (15.24 cm) planes is 1 nSec. One wavelength will stand in the resonant cavity at 1 GHz. One half wavelength will stand in the cavity at 500 MHz and the quarter wave length frequency is 250 MHz. Just like transmission lines, multiples of half wavelengths (1, 3/2, 2, 5/2, ...)are responsible for the peaks and multiples of quarter wavelengths (3/4, 5/4, 7/4, 9/4, ...) are responsible for the dips in impedance. As the frequency increases, the magnitude of the peaks and dips diminishes because frequency dependent loss (skin and dielectric) increases with frequency and the Q of the resonant cavity drops because of loss. This is discussed further in section IV.

Figure 3b shows how a time domain step propagates along the plane. When the step hits the open circuit edge at the far end of the planes, it doubles and reflects back. The delay for the step is the same as that of a single transmission line, about 170 pSec per inch (66.93 pSec per cm) in material. The time delay for the RLC components and the SPICE T-elements are similar but the delay for the W-element is about 8.6% longer. This is because the frequency dependent loss is

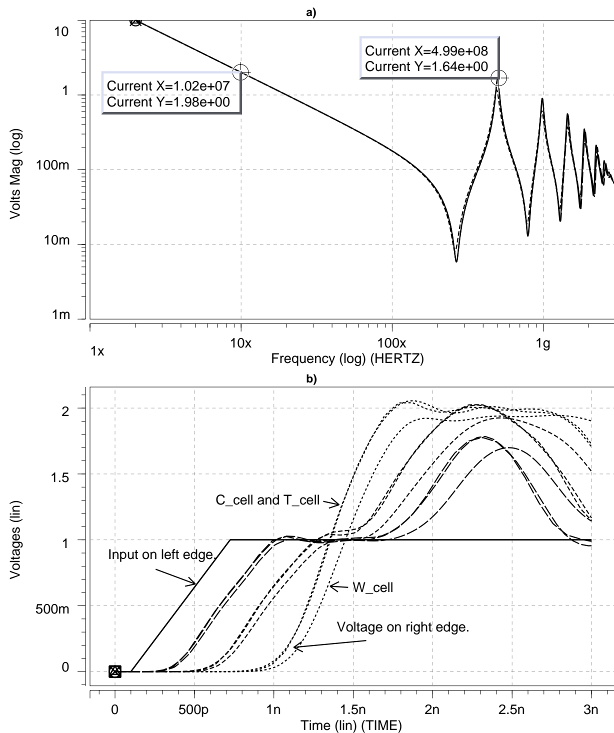

Figure 3: Power planes stimulated from left edge. a) Frequency domain simulation. The C_cell, T_cell and W_cell give similar results. b) Time domain simulation. Only the W_cell has correct frequency dependent loss which results in waveform attenuation.

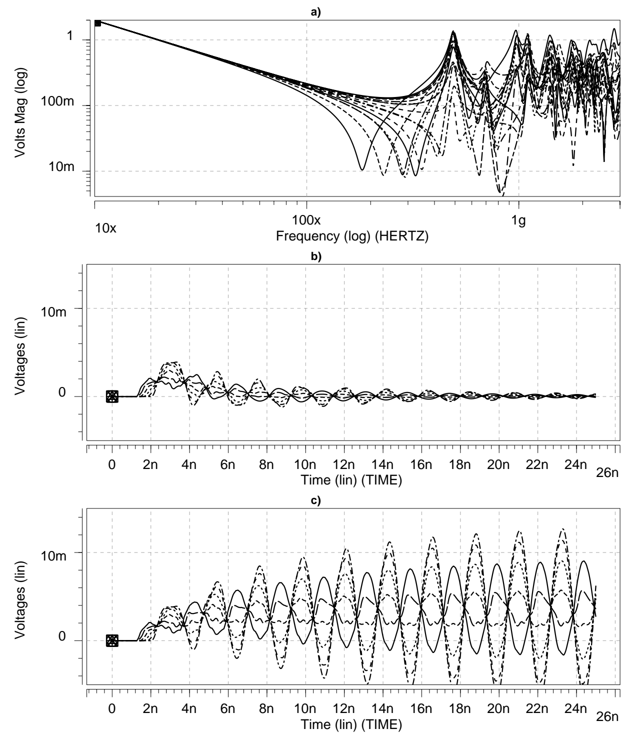

Figure 4: Stimulation from a point source on the planes. a) Frequency domain. b) Single pulse in the time domain. c) 500 MHz pulse train. Continual stimulation at the resonant frequency slowly builds up the resonance.

correctly modeled for the W element but is not accounted for with the C_cell and T_cell. The rise time degradation due to skin and dielectric loss is obvious after the wavefront has crossed the power planes to the right hand side. There appears to be an additional delay for the W_cell waveform but it is not due to a velocity difference. Attenuation of higher frequency has the appearance of additional delay.

By stimulating the edge of the plane, it is apparent that the C_cell, T_cell and W_cell produce the correct capacitance at low frequency and the correct cavity resonances at higher frequency. Only the W_cell gives correct results in the time domain because the other cells do not account for frequency dependent loss.

Stimulation from a single point

Figure 4a shows a more realistic case where the same power planes stimulated with 1 AC amp injected between the planes from a single point rather than the whole left hand side. The several traces are the voltages measured between the vertical nodes at several of the 64 positions on the power planes and represent the transfer impedance at those nodes. Nearly all of the nodes have peaks at the frequencies associated with multiples of a half wavelength as determined by the length and width dimensions of the power planes. The dips occur at many different frequencies because they are associated with quarter wavelength multiples from the measurement point to an open edge of the planes. At frequencies well below the first resonant dip, all points on the board are at the same voltage. Components placed anywhere on the planes will see nearly the same voltage measured across the power planes. But at higher frequencies (above the first resonant dip), position on the planes becomes very important.

In figure 4b, the same power planes have been stimulated from the same point by a single time domain pulse. The several traces are at adjacent points along the plane in one direction. The time delay between points is apparent. Figure 4c shows the same simulation on the same scale, but with a 500 MHz pulse train which matches the first impedance peak determined in the frequency domain analysis. The first pulse does not create much disturbance. But as pulses continue to reinforce each other at a resonant frequency, each pulse puts a little more energy into the cavity. Cavity resonances build up until the losses due to conductor resistance, skin effect and dielectric loss balance the energy that is delivered by the source. The first pulse flows out from the source in a radial fashion. But as time goes on and each pulse reflects off the edges of the planes, the wave fronts are no longer radial but become plane waves perpendicular to the square edges of the planes. Power plane resonances are associated with plane waves bouncing off the rectangular edges of the power planes. Irregular shaped power planes will not have the high Q peaks and dips associated with rectangular shaped planes because plane waves do not build up on irregular shapes, although other resonances are possible (i.e. circular shaped planes).

One of the major purposes for this type of power plane analysis is to identify the magnitude and frequency of the peaks and dips caused by resonances associated with cavity dimensions. For planes with parallel edges, the peaks and

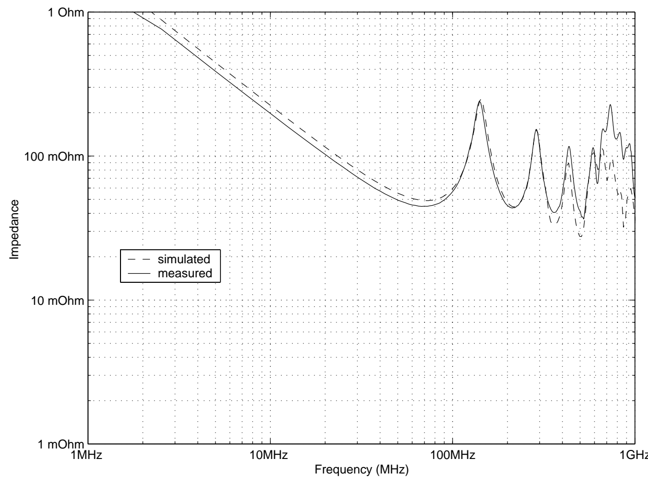

Figure 5: Simulated and measured power plane impedance in the frequency domain.

dips are associated with plane waves and are well represented by orthogonal transmission line segments. This justifies the plane wave assumptions that were made in the parameter calculations in section II above and the use of orthogonal elements in the model. Circular and irregular shaped planes may not be as well represented by this technique.

Hardware Measurements

Model to hardware correlation is obtained in the frequency domain by using a vector network analyzer (VNA) and making S21 measurements [10]. Calibration is done by soldering the 50 ohm coaxes of port 1 and port 2 together with no DUT. The "through" calibration is set to 0 dB. The parallel combination of the two coaxes is 25 Ohms, which becomes the reference impedance. A bare printed circuit board with no attached components is used for the measurements. Port 1 and Port 2 are attached to the power planes through decoupling capacitor pads at distant points on the board by soldering down the 50 ohm coax probes with short connections. The VNA gives S21 readings in dB, which are converted to impedance by the equations

$$|S21| = 20\log_{10}\frac{|Z_{plane}|}{25} \quad \text{and} \quad |Z_{plane}| = 25\cdot 10^{\frac{|S21|}{20}} \tag{10}$$

Figure 5 shows good correlation for the simulated and measured frequency domain impedance of a 20x10 inch (50.8 cm x 25.4 cm) pair of power planes with 2 mils (50.8 mm) separation. The same power planes are driven with a time domain pulse generator at the same positions. The pulse generator drove 0 volts for a long time and then a square wave at 140 MHz, one of the resonant peaks from the frequency domain measurements. Figure 6 shows the time domain simulated and measured results. Figures 5 and 6 show hardware confirmation of the concepts presented in figure 4. The power plane SPICE models have good model to hardware correlation in both the frequency and time domains.

This section has demonstrated the use of power plane HSPICE models. Accuracy has been verified by comparison to known capacitance values, one dimensional cavity resonances which are easily calculated and finally by correlation to measured hardware. Much insight has been gained into the nature of power plane cavity resonance and

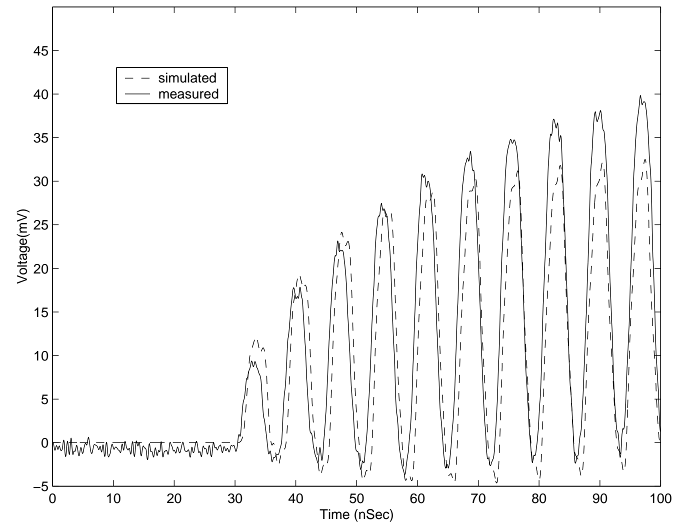

Figure 6: Simulated and measured time domain response. Planes are repetitively stimulated at the resonant frequency. Noise on planes builds up until the energy lost equals the energy gained on each cycle.

the importance of frequency dependent loss through simulation of the models.

IV. Materials and Geometries

The HSPICE power plane model is now used to compare the properties of power planes with different materials and geometries. It is desirable to make the power planes low impedance over as wide of a frequency range as possible. This section describes the role of the dielectric thickness, dielectric constant and the results of several pairs of power planes in parallel. Once again, the planes are stimulated along the left hand edge with a 1 amp current source so that the cavity resonances are clearly recognizable.

Figure 7a shows simulation results for the same 6 inch (15.24 cm) square power planes with dielectric thickness of 0.25, 1, 4, and 16 mils (6.35 mm, 25.4 mm, 101.6 mm, and 406.4 mm). Impedance of the capacitive portion of the curve is reduced proportionally to the dielectric thickness, as expected from equation 1. The cavity resonant frequencies have not changed because the velocity through the dielectric is proportional to the dielectric constant which has not changed (equation 2).

The amplitudes of the resonances are reduced as the dielectric thickness is reduced [11] [12]. The Q of the resonant circuit is related to the loss. The loss factor for a low loss transmission line is [13]

$$\alpha = \frac{R}{2Z_0} + \frac{G\,Z_0}{2} \tag{11}$$

where Z_0 is the characteristic impedance of the transmission line and R and G are the series conductive and parallel dielectric loss values as defined in equations 6 and 7. This formula applies to power planes because the planes are modeled as an array of lossy transmission lines. The power planes are low loss because $R << \omega L$ for the frequencies of interest and $G << \omega C$ with low loss tangent materials.

As dielectric thickness decreases, skin effect resistance remains constant. But the characteristic impedance defined in equation 4 is proportional to the thickness because inductance and capacitance are proportional and inversely proportional to

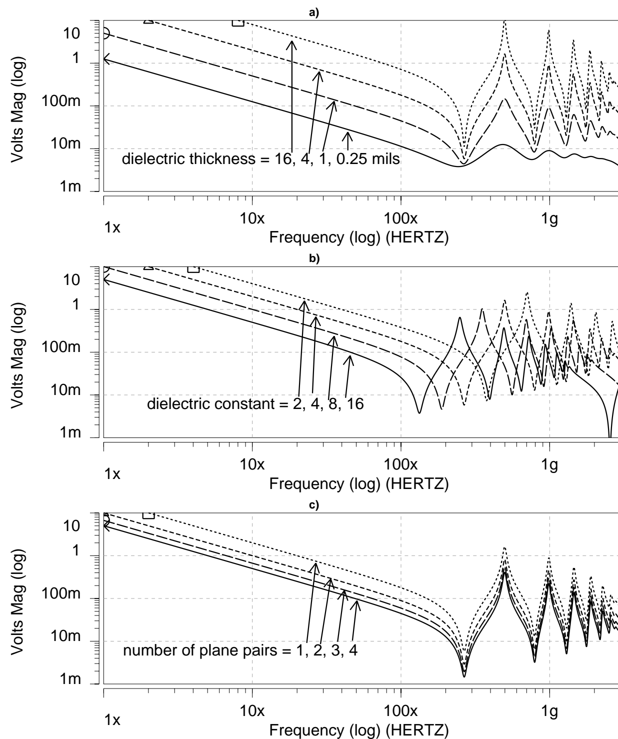

Figure 7: Comparison materials and geometries for power planes. a) Dielectric thickness. b) Dielectric constant. c) Number of power plain pairs in parallel. Thin dielectrics are most effective in reduction of plane impedance and noise.

the dielectric thickness respectively. The first term of equation 11 is inversely proportional to the dielectric thickness and is responsible for the damping out of the cavity resonances with thinner dielectric. The second term is constant with thickness. Thin dielectrics between power planes offer a tremendous advantage in designing low impedance and low noise power distribution systems.

Figure 7b shows the simulation results for dielectric constants of 2, 4, 8 and 16. The increase in dielectric constant increases the capacitance of the planes and the low frequency part of the curve is reduced in impedance accordingly. The cavity resonant frequencies have all changed because the velocity through the dielectric goes as $1/\sqrt{\epsilon_R}$. The cavity resonances have damped out somewhat because capacitance has increased but the inductance of the structure has not changed. An increase in dielectric constant helps to reduce the impedance and cavity resonance amplitudes somewhat, but is not as effective as a reduction in dielectric thickness.

Pairs of power planes in parallel are simulated by two equivalent methods and achieve identical results. Since SPICE node zero is not part of the power plane topology, pairs of power planes may be stacked on top of each other by simply connecting the top nodes of one pair of power planes to the bottom nodes of the next pair of planes. Conductive layers may alternate between Vdd and Vss. All Vdd planes and all Vss planes of the stackup are connected together at each via point.

A simpler approach is to recognize that the capacitance of power plane pairs in parallel is increased over the capacitance of a single power plane pair. Two pairs of power planes with 4 mil dielectric have the same capacitance as a single pair of power planes with 2 mil dielectric, assuming the same dielectric constant. In general, the equivalent thickness of *n* power plane pairs in parallel is

$$t_{equivalent} = \frac{1}{\frac{1}{t_1} + \frac{1}{t_2} + \ldots + \frac{1}{t_n}} \qquad (12)$$

where t is the thickness of the dielectric. The velocity and cavity resonant frequencies are correct because the dielectric constant has not changed. But with the simpler method, care must be taken to correctly account for conductor resistance by accounting for the total thickness of copper and the number of skin effect layers in parallel. The simpler method also assumes that many low inductance vias have been used to connect the power plane pairs in parallel. If via inductance is important, then power planes should be stacked as described above and connected with inductors.

Figure 7c shows the simulation results with 1, 2, 3 and 4 pairs of power planes in parallel. The impedance is linearly reduced in all portions of the impedance vs frequency curve. There is no reduction in cavity resonance amplitude as there was with thinner dielectric because there are more skin surfaces to carry current.

Dielectric thickness, dielectric constant and multiple planes in parallel will all reduce the impedance of power planes. Of the three techniques, thin dielectric is the most effective because it gives the greatest damping at high frequency.

V. Spreading Inductance

Spreading inductance is given in equation 3 and discussed as a material property with units of henrys per square. It is proportional to dielectric thickness and is a result of magnetic field stored between the power planes as equal currents of opposite direction flow on the Vdd and Vss power planes. It is important because it contributes to the mounted inductance of both decoupling capacitors and silicon circuits. Power plane spreading inductance is likely to be the dominant inductance (impedance) between a micro processor chip and the decoupling capacitors that supply high frequency current to the chip. It is most responsible for the inductance that contributes to chip-package resonance [14]. It also contributes to the mounted inductance of decoupling capacitors [15]. This section discusses the power plane spreading inductance associated with mounted decoupling capacitors on physical hardware and in SPICE simulation.

Decoupling capacitors are usually connected to the power planes with low inductance vias. The mounting loop inductance is measured by using a shorting bar resonance technique [16]. A strap of metal is soldered across the capacitor mounting pads to short circuit the Vdd and Vss power planes. No capacitor is present. The measured inductance comes from the loop that current makes as it flows on a Vdd power plane into the vicinity of the vias, around the via-pad-shorting bar loop, and then away from the vias on the Vss power plane. The power planes are driven with a vector network analyzer and an S21 measurement is made as described in section III. A parallel tank circuit is formed by

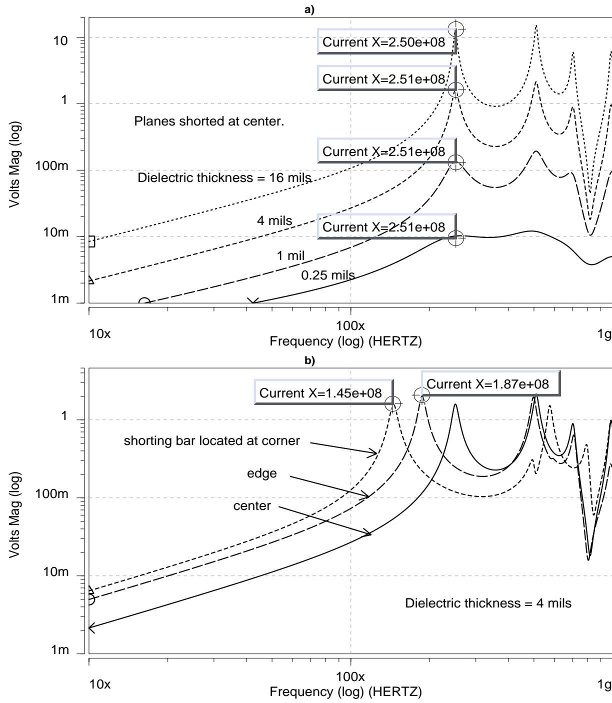

Figure 8: The Vdd and Vss planes are connected with an ideal short circuit in SPICE simulation. The frequency of the first peak is determined by the plane capacitance and short inductance. a) Power planes with 16, 4, 1 and 0.25 mil (6.3, 25, 101, and 406 mm) dielectrics. b) Shorting bar placed at center, edge and corner of power planes.

the capacitance of the power planes and the inductance of the shorted decoupling capacitor pads. There is a peak in the measured impedance curve at frequency

$$f_0 = \frac{1}{2\pi\sqrt{L \cdot C}} \qquad L = \frac{1}{(2\pi f_0)^2 C} \tag{13}$$

The power plane capacitance C and resonant frequency f_0 are easily measured and total inductance L for the mounting structure is calculated .

In a similar way, simulation is used to find power plane spreading inductance in HSPICE. The power planes are shorted together vertically with an ideal short. Current jumps from the Vdd plane to the Vss plane through an ideal voltage source with 0 volts. The resonant peak observed in SPICE is a result of the power plane capacitance and spreading inductance. Just like the physical measurement, equation 13 is used to find the inductance in SPICE. But in simulation, there is no inductance contribution from the vias and pad structures and the power plane inductance is isolated. This is the partial mounting inductance due to power plane spreading inductance for the decoupling capacitor loop.

Figure 8a shows the simulation results of a pair of power planes with an ideal short between them, located in the center of the planes. Simulations are run with 0.25, 1, 4 and 16 mils (6.3, 25, 101, and 406 mm) of dielectric thickness. The peak due to the parallel capacitance and inductance is at the same frequency, independent of the dielectric thickness. Capacitance is inversely proportional to dielectric thickness and power plane inductance is proportional to thickness so the peak frequency is independent of the thickness. Table 2

Dielectric Thickness (mils)	Resonant Frequency (Mhz)	Plane Capacitance (nF)	Calculated Inductance (pH)
16	250	2.0	200
4	251	8.1	50
1	251	32.4	12
0.25	251	129.6	3

Table 2: Power plane inductance for planes with several different dielectric thicknesses.

shows a dramatic reduction in the power plane inductance calculated for each plane pair when thin dielectrics are used.

Figure 8b shows the simulation results of a pair of 4 mil (101 mm) dielectric power planes that are shorted at 3 different points. The resonant frequency changes depending on whether the planes are shorted at the center, side or corner of the printed circuit board. The corner is found to have the highest spreading inductance. This is because current has four directions (north, south, east and west) to feed into and escape from the short at the center of the board, three directions to escape at the side of the board, and only two directions to escape at the corner of the board. Inductance increases when current is forced to escape in a smaller section of the plane pair. Table 3 gives the power plane spreading inductance for three positions on the board.

Plane Position	Resonant Frequency (Mhz)	Plane Capacitance (nF)	Calculated Inductance (pH)
Center	250	8.1	50
Edge	187	8.1	89
Corner	145	8.1	149

Table 3: Power plane spreading inductance for 3 different positions on a printed circuit board.

From these simulations it is apparent that spreading inductance is a strong function of dielectric thickness and position on the power planes. It is minimized by using thin power plane dielectric and keeping components in the center of the board. This important result applies to mounted silicon chips as well as mounted capacitors.

Hardware Measurements

The power plane simulation results are confirmed with hardware measurements. Figure 9 shows Simulated and measured results for a power plane pair with and without a shorting bar. Without the shorting bar, the power planes with 2.9 mils (73 mm) of dielectric have 15.1 nF of capacitance. The simulated power plane impedance closely matches the measured impedance up to nearly 1 GHz.

When shorted by a strap soldered across the decoupling capacitor pads, the hardware structure has a resonant peak at 67.2 MHz. The total loop inductance measured for the power planes, vias and mounting pads is

$$L = \frac{1}{(2\pi f_0)^2 C} = \frac{1}{(2\pi\ 67.2\ MHz)^2\ 15.1\, nF} = 371\ pH \tag{14}$$

SPICE is then forced to match the measured frequency peak by choosing an inductance that causes a simulation peak to appear at the same frequency as the measured peak. The inductance chosen is 324 pH, somewhat less than the

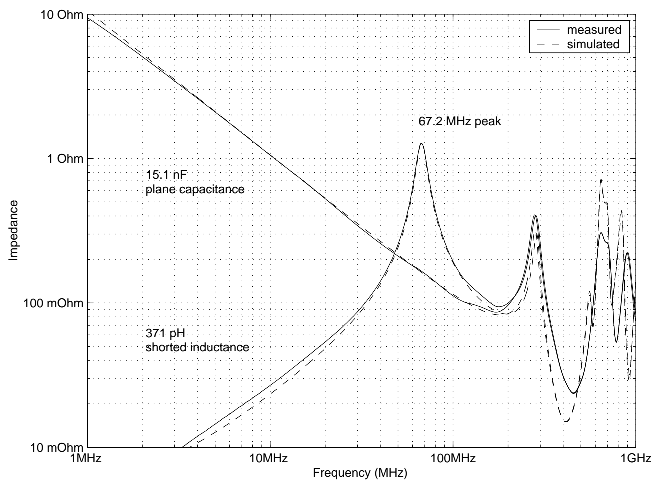

Figure 9: Simulated and measured shorting bar soldered on decoupling capacitor pads. Capacitance of power planes resonates with inductance of power planes, pads and vias. The total mounting inductance is 371 pH.

measured value. When the simulated power planes are shorted with an ideal short in SPICE, the resonant frequency is 174 MHz and the partial inductance calculated for the power planes using equation 14 is 55 pH. The sum of the partial power plane inductance and the inductance chosen to force SPICE to match hardware measurements is 324 + 55 = 379 pH, very close to the 371 pH found by hardware measurement. The explicit inductance chosen to make SPICE simulation match hardware measurements is consistent with finite element extraction of the loop inductance for the vias and shorting bar structure alone. Power plane spreading inductance is an important part of the mounted inductance for decoupling capacitors and silicon chips. The power plane model correctly accounts for spreading inductance in simulation.

Conclusions

Low power plane impedance at high frequency is important for the power distribution systems of modern computers. A method of simulating the power planes in SPICE has been presented. Unit cells based on lumped RLC elements, ideal transmission lines and lossy transmission lines have been demonstrated, each with their own advantages and disadvantages. Accuracy of the models has been checked by comparing simulated results with known values of capacitance and one dimensional cavity resonances. Model to hardware correlation has been shown in the frequency and time domains.

The SPICE model was used to examine the role of dielectric thickness, dielectric constant and the number of planes in parallel. Thin power plane dielectric was found to be the most effective way to reduce power plane impedance and noise. Power plane spreading inductance is part of the total inductance associated with a mounted decoupling capacitor and silicon chip. The spreading inductance is proportional to dielectric thickness and depends upon the location on the board. It is simulated or measured by shorting the power planes together and measuring a parallel resonant frequency. Good model to hardware correlation has been shown for spreading inductance.

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