Agenda

- PDN Overview and Measured Responses
- PDN Equations
  - Frequency Domain
    - Target impedance
    - Resonant peak
  - Time Domain
    - Transient currents
    - Clock edge
    - Time average
- Time Domain Responses
  - Impulse
  - Step
  - Resonance
- Which comes first, voltage or current?
- Switched Capacitor Load
- Responses to CMOS loads
Components for Power Distribution Network (PDN)

\[ Z_{\text{target}} = \frac{V_{dd} \times \text{tolerance}}{I_{\text{max}} - I_{\text{min}}} = \frac{1.2 \times 0.05}{7A - 2A} = 10 \text{ mOhm} \]

PDN resonance

PMIC
bulk cap
high frequency caps
die cap
System Cross Section

- Die on Package on PCB
- Capacitance is mostly on the die
- Inductance is mostly in the package and PCB
- Resistance is in the die, package, PCB and capacitors
- Simple RLC circuit closely represents system
- Next we will examine lab measurements for a real hardware system
PDN Impulse Response

- FPGA circuits switched only once
  - Single clock edge
  - One impulse of clock edge current
  - Impulse response signature

- Fall time is 300ps
  - All charge must come from on-die capacitance

- Initial voltage sag:
  \[ \Delta V = \frac{Q_{\text{clock edge}}}{C_{\text{odc}}} \]

- System PDN responds to “impulse” of current
  - Damped sinusoid at resonant frequency

- On-die PDN noise is much higher than PCB PDN noise
  - 172 mV p-p
  - 105 mV sag
**PDN Step Response**

- **Burst of impulses**
  - Many impulses
    - Clock edge current
  - Package current ramps up
  - PDN transient response
    - Damped sinusoid
- **PDN responds when clock stops**
  - Inductance drives current into die capacitance
  - PDN response with damped sinusoid
- **Clock gating**
  - \( F_{\text{clock}} = 266\text{MHz} \)
  - Modulate at any frequency
- **Core voltage**
  - Droop: 146mV
  - Pk-pk: 228mV
    - Larger than impulse (172 mV)
PDN Resonance Response

- Clock gating
  - $F_{\text{clock}} = 533$ MHz
  - $F_{\text{gate}} = 33$ MHz

- Step transients repeat at PDN resonant frequency 33MHz

- Known as “Resonance Response”
  - AKA “periodic burst transient”

- 577mV pk-pk PDN noise
  - 1.1V nominal supply
  - +/- 26% supply...

- Worst case PDN noise
  - Will not happen under normal operation
  - Clock gating can cause this
  - Power gating can cause this
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Target Impedance Definition

- Based on Ohms Law
- Two easily understood and difficult to obtain parameters
  - Tolerance
  - Transient current
    - Can be expressed as percentage of maximum current
- Target impedance is a function of frequency if
  - Tolerance is a function of frequency
  - Transient current is a function of frequency

\[
Z_{\text{target}} = \frac{Vdd \times \text{tolerance}}{I_{\text{max}} - I_{\text{min}}} = \frac{1.2 \times 0.05}{7 \times 2} = 10 \, \text{mOhm}
\]

Supply that meets \(Z_{\text{target}}\) almost certainly will not exceed specified voltage tolerance with given transient current

... but that can be expensive ...
Equations for Series and parallel circuits

- Measure series resonance from the FPGA balls
- Simulate parallel resonance from FPGA circuits
- The RLC elements are the same

Resonant frequency

$$f_0 = \frac{1}{2\pi \sqrt{LC}}$$

Reactance at resonance

$$X = Z_0 = \sqrt{\frac{L}{C}}$$

$$Q\text{-factor} = \frac{Z_0}{R} = \frac{\sqrt{L/C}}{R}$$

Estimate of impedance peak at resonance

$$Z_{peak} \approx Z_0 \cdot Q\text{-factor} = \frac{X^2}{R} = \frac{L/C}{R}$$
PDN Parameter Calculations – Frequency Domain

- Spread Sheet for PDN parameter calculations
  - Inputs (independent parameters) are the green shaded cells
  - Results (dependent parameters) are calculated in the white cells

- Desire 100 mOhm peak at 100 MHz
  - Choose 50 nF for on-die capacitance
  - Calculate \( L \)
    \[ f_0 = \frac{1}{2\pi} \sqrt{LC} \]
  - Calculate \( Z_0 \)
    \[ Z_0 = \sqrt{L/C} \]
  - Calculate q-factor
    \[ q\text{-factor} = \frac{Z_0}{R} = \frac{\sqrt{L/C}}{R} \]
  - Choose \( R \) for 100mOhm peak
    \[ Z_{\text{peak}} = Z_0 \times q\text{-factor} = \frac{L/C}{R} \]

<table>
<thead>
<tr>
<th>Frequency Domain</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vdd</td>
</tr>
<tr>
<td>Core Cap</td>
</tr>
<tr>
<td>PDN loop Inductance</td>
</tr>
<tr>
<td>PDN loop resistance</td>
</tr>
<tr>
<td>dynamic current</td>
</tr>
<tr>
<td>Resonant Frequency</td>
</tr>
<tr>
<td>PDN ( Z_0 )</td>
</tr>
<tr>
<td>q-factor from PDN loop</td>
</tr>
<tr>
<td>Expected impedance Peak</td>
</tr>
<tr>
<td>Target Impedance</td>
</tr>
<tr>
<td>Assumed Die resistance</td>
</tr>
<tr>
<td>External PDN loop resistance</td>
</tr>
</tbody>
</table>

- Impedance (Ohms)

- On-die capacitance
- Inductance
- Dynamic current
- Resonant Frequency
- PDN loop resistance
- Assumed Die resistance
- External PDN loop resistance

- On-die capacitance
- Inductance
- Dynamic current
- Resonant Frequency
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Transient Current Considerations

- **Transient current paradox**
  - Commonly used terminology
  - But often misunderstood…

- **Examples of Transient current**
  - Impulse: Clock edge current
  - Step: Burst transient
  - Resonance: Periodic burst transient

- \( I_{\text{transient}} = I_{\text{max}} - I_{\text{min}} = \Delta I \)

- **Current waveforms have large variation across system**
  - Filtering effect of inductance and capacitance
  - Very different time constants

- **Current profiles have frequency content depending on length of time, \( dt \)**
  - 100’s of pSec only affects die
  - Few nSec affects package
  - 10’s of nSec affects PCB
  - \( \mu \)Sec affects VRM
Current Definitions – On-Chip Level

- **Clock edge current:**
  - **Instantaneous** current drawn by die logics at clock edges

- **Charge per clock cycle:**
  - Independent of clock frequency
  
  \[ Q = \int_0^T i_{\text{clk}_\text{edge}}(t) \cdot dt \]

- **Dynamic current:**
  - **Time averaged** clock edge current
  - Comes with the clock
  - Static (leakage) current not included
  - Used for target impedance design
  - Proportional to clock frequency

  \[ I_{\text{dynamic}} = \frac{Q}{T} = \frac{1}{T} \int_0^T i_{\text{clk}_\text{edge}}(t) \cdot dt \]
System level current considerations

Low Activity:
- Clock is active but Data is Idle

High Activity:
- Clock and Data are active

Transient Current:
- High-activity dynamic current minus low-activity dynamic current
- AKA power transient

**System Level PDN responds to power transients. Clock edge currents are filtered by the package.**
PDN Parameter Calculations – Time Domain

- Dynamic current is easily calculated
  - Average bench current
  - Clock frequency
  - Assumes all clock cycles are equal
  \[ Q_{cycle} = \frac{I_{dynamic}}{f_{clock}} \]

- Each average clock cycle consumes this amount of charge

- Charge is consumed from on-die capacitance
  \[ Q = CV \]
  \[ dQ = C \cdot dV \]

- Impulse response (droop) from single clock cycle
  \[ V_{clock\ edge} = \frac{Q_{cycle}}{OC} = \frac{I_{dynamic}}{f_{clock}} = \frac{1.55A/1GHz}{50nF} = 31mV \]

- Step response (droop) from fast edge
  \[ V_{step} = I_{step} \cdot Z_0 = 1.55A \cdot 32mOhm = 49mV \]

- Resonance response (peak-peak) from repeating steps
  \[ P-P_{resonance} = 4 \cdot I_{tran} \cdot Z_{peak} = 4 \cdot 1.55A \cdot 100m\Omega = 198mV \]

### Frequency Domain

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vdd</td>
<td>1 V</td>
</tr>
<tr>
<td>Core Cap</td>
<td>50 nF</td>
</tr>
<tr>
<td>PDN loop Inductance</td>
<td>50.7 pH</td>
</tr>
<tr>
<td>PDN loop resistance</td>
<td>10.1 mOhm</td>
</tr>
<tr>
<td>Resonant Frequency</td>
<td>100 MHz</td>
</tr>
<tr>
<td>PDN Z_0</td>
<td>32 mOhm</td>
</tr>
<tr>
<td>q-factor from PDN loop</td>
<td>3.15</td>
</tr>
<tr>
<td>Expected impedance Peak</td>
<td>100 mOhm</td>
</tr>
<tr>
<td>Target Impedance</td>
<td>32 mOhm</td>
</tr>
<tr>
<td>Assumed Die resistance</td>
<td>5.0 mOhm</td>
</tr>
<tr>
<td>External PDN loop resistance</td>
<td>5.1 mOhm</td>
</tr>
</tbody>
</table>

### Time Domain

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>f_{clock}</td>
<td>1.55 GHz</td>
</tr>
<tr>
<td>charge per clock cycle (Q_{cycle})</td>
<td>1.55 nCoul</td>
</tr>
<tr>
<td>Expected clock edge droop (impulse)</td>
<td>31 mV</td>
</tr>
<tr>
<td>Expected step response droop</td>
<td>49 mV</td>
</tr>
<tr>
<td>Expected peak-peak noise at resonance</td>
<td>198 mV</td>
</tr>
</tbody>
</table>

\[ PDN \ Z_0 = \sqrt{\frac{L}{C}} \]
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Impulse Response – PWL Current Source

- Impulse of charge is consumed from PDN
  \[ Q = \frac{I_{\text{dynamic}}}{f_{\text{clock}}} \]

- Happens in less than 1 clock cycle
- Calculate droop from \( Q = CV \)
  \[ V_{\text{droop}} = \frac{I_{\text{dynamic}} / f_{\text{clock}}}{ODC} = \frac{1.55 A / 1 \text{GHz}}{50 \text{nF}} = 31 \text{mV} \]

- Simulated Droop
  - 29 mV
  - Some current came in during impulse

- Droop is determined by on-die capacitance
  - Inductance has no effect
  - Impedance peak has no effect

Convention: Current into a circuit element is positive
Step Response and Characteristic Impedance - Transient

- PDN parameters chosen so that
  \[ Z_{\text{target}} = Z_0 = \sqrt{L/C} \]

- PDN Parameters
  - \( V_{\text{dd}} = 1\, \text{V} \)
  - \( I_{\text{transient}} = 1.55\, \text{A} \)
  - Tolerance = 5%
  - Cap = 50 \, \text{nF}
  - Inductance = 50.7 \, \text{pH}

- Step Response Droop
  - 50 mV
  - Same as 5% tolerance

\[ Z_{\text{target}} = \frac{V_{\text{dd}} \times \text{tolerance}}{I_{\text{transient}}} = \frac{1 \times 5\%}{1.55} = 32 \, \text{mOhm} \]

\[ Z_0 = \sqrt{\frac{L}{C}} = \sqrt{\frac{50.7 \, \text{pH}}{50 \, \text{nF}}} = 32 \, \text{mOhm} \]

Make \( Z_0 = Z_{\text{target}} \) in order to have step response droop = tolerance
Resonance Response

- Estimate P-P noise
  - $Z_{\text{peak}}$ is 103 mOhms
  - $I_{\text{tran}} = 1.55A$ pulses for 5 nSec

$$PP_{\text{resonance}} = \frac{4}{\pi} I_{\text{tran}} Z_{\text{peak}}$$

$$= \frac{4}{\pi} 1.55A \times 103m\Omega$$

$$= 203mV$$

- The $4/\pi$ comes from Fourier transform of square wave

- Simulated P-P noise
  - 201 mV

- Mitigate resonant peak by
  - Reducing L
  - Increasing C
  - Increasing R (damping)
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Current, Voltage and Time for Reactive Components

- **Capacitor**
  - Voltage lags behind current
    - Current into capacitor changes voltage
    \[ \frac{dv}{dt} = \frac{I}{C} \quad V = \frac{1}{C} \int I \cdot dt \]
    - I/C is the forcing function
    - dv/dt is the result

- **Inductor**
  - Voltage leads current
    - Voltage across inductor changes current
    \[ \frac{di}{dt} = \frac{V}{L} \quad I = \frac{1}{L} \int V \cdot dt \]
    - V/L is the forcing function
    - di/dt is the result
Transient Current, Rise Time and $\frac{di}{dt}$

- If $\frac{di}{dt}$ is a result of $V/L$...
- Then why do we often consider $\frac{di}{dt}$ to be the enemy, the cause of PDN noise?
  - The “small-signal” ratio of $\frac{di}{dt}$ is not the problem
- The “large-signal” transient current is the problem ($dl$)
  - A larger transient current contains more noise energy and requires lower impedance
- A short time span ($dt$) makes the problem worse
  - Raises the frequency of the noise.
  - May stimulate high frequency impedance peak if it is fast enough
  - $dt$ determines the portion of the PDN that will supply the current
    - VRM, board capacitors, package capacitor, On-die capacitance
- $dl$ and $dt$ are independent parameters and should not be considered to be a ratio
  - Large $\frac{di}{dt}$ is associated with low inductance and is a good thing
- Single clock edge creates impulse
- Sequence of Events
  - Circuits consume die current (charge)
  - Die voltage droops
  - Current comes in from outside inductor
    - Brings voltage back to nominal
  - Current diminishes as die voltage rises above nominal
- Inductor current ramps up until die voltage returns
- Current into die capacitance leads die voltage

Inductor current responds to voltage across it (voltage leads current)

Die capacitor voltage lags behind inductor current
Cut PDN inductance in half
- 25.35 pH
  - down from 50.7 pH

Charge consumed from die is constant

Inductor \( \frac{di}{dt} \) doubles
- Slope is twice as steep
- Current ramps up faster

Initial droop is the same
- Resonant frequency is higher
- \( q \)-factor is lower

\( \frac{di}{dt} \) is the inductor response to \( V/L \)
Key Concepts for PDN on-die capacitance and inductor

- The on-die voltage can only be changed by passing current through the capacitance

- The root cause of PDN voltage noise is charge drawn from the on-die capacitance
  - The on-die voltage noise is inversely proportional to $C$
  - The voltage noise during the clock cycle is determined by the charge (integral $I \times dt$)

\[
V = \frac{1}{C} \int I \cdot dt
\]

- Inductor current does not come in from the outside world until the die voltage drops
  - Current through the inductor remains constant until a voltage appears across it
  - A smaller inductor makes a higher $\frac{di}{dt}$ and brings current in faster (this is good)

\[
\frac{di}{dt} = \frac{V}{L}
\]
\[
I = \frac{1}{L} \int V \cdot dt
\]
Take-Aways

- Increase the die capacitance to reduce the voltage noise
  - Fast PDN noise droops are proportional to $1/C$

- Reduce the system inductance to bring current (charge) into the die faster
  - Incoming current reduces the charge delivered by the on-die capacitance

- Both of these are costly
  - But you get what you pay for
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Time Domain Load Circuit

• Previous Loads
  – Current source
    • Current is independent of voltage
    • Provides no damping
  – Time varying resistor
    • Current diminishes with less voltage
    • Provides damping

• New Load Circuit
  – Operates the same way as CMOS circuits
    • Current is proportional to voltage
    • Provides damping
  – Portion of the ODC is switched
    • Switch factor
  – Easily handles power transients
    • Load capacitance changes with time
    • Take some capacitance from the load and put it back into ODC
Load Operation

- **Switch low-to-high**
  - Current charges lower cap
  - Upper cap discharges
- **Switch high-to-low**
  - Current charges upper cap
  - Lower cap discharges
- **Resistor sets time constant**
  - 2x current for each edge
  - Reverses direction for each edge
  - 1x current drawn from ODC for each edge
- **Switch factor**
  - Calculated in spread sheet
  - Draws dynamic current from package
  - Expressed as percentage of ODC
- **Transient current**
  - Load capacitance varies with time
  - Example: draw 8 amps at 500 MHz (max current)
    - 10% of ODC is placed in load cap position
    - A 50% current transient is desired (draw 4 amps)
    - Load cap is reduced by half to 5% of ODC
    - Clock frequency remains the same but 4 amp transient has occurred
- **Real CMOS circuits operate this way**
Load Waveforms

- Load voltage alternates between 0V and 1V (red)
- 2x Current is drawn through resistor both directions (blue)
- 1x Current is drawn from ODC on each edge (green)
- Events
  - 10nSec: load starts
  - 20nSec: load drops in half
  - 30nSec: back to full load
    - 10% switching factor
  - 40nSec: half load
    - 5% switching factor
- Load capacitance changes with time
- Time constant is set with resistor
Calculate Switch Activity from $Q=CV$

- One Clock Edge
  - PDN Impulse Response
- Initial voltage sag:
  \[ \Delta V = \frac{Q_{\text{clock}_{\text{edge}}}}{C_{\text{odc}}} \]
- Calculate **average** clock edge charge
  \[ q_{\text{edge}} = \frac{\text{current}}{\text{frequency}} = \frac{10 \text{ amp}}{533 \text{ MHz}} = 18.8 \text{ nCoul} \]
- Calculate the capacitance that must have switched
  \[ C_{\text{switched}} = \frac{q}{V} = \frac{18.8 \text{ nCoul}}{1.1 \text{ V}} = 17.1 \text{ nF} \]
- Calculate the switch factor given the on-die capacitance
  \[ S.F. = \frac{q_{\text{switched}}}{ODC} = \frac{17.1 \text{ nCoul}}{300 \text{ nCoul}} = 0.057 = 5.7\% \]
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Impulse Response – Switched Capacitor Load

- Impulse of charge is consumed from PDN
  \[ Q = \frac{I_{\text{dynamic}}}{f_{\text{clock}}} \]
- Happens in less than 1 clock cycle
- Calculate droop from \( Q = CV \)
  \[ V_{\text{droop}} = \frac{I_{\text{dynamic}}/f_{\text{clock}}}{ODC} = \frac{1.55A/1\text{GHz}}{50nF} = 31mV \]
- Simulated Droop
  - 29 mV
  - Some current came in during impulse
- Droop is determined by on-die capacitance
  - Inductance has no effect
  - Impedance peak has no effect
Step Response and Characteristic Impedance - Transient

- PDN parameters chosen so that
  \[ Z_{target} = Z_0 = \sqrt{L/C} \]

- PDN Parameters
  - \( V_{dd} = 1V \)
  - \( I_{transient} = 1.55A \)
  - Tolerance = 5%
  - \( C = 50 \text{ nF} \)
  - Inductance = 50.7 \text{ pH} 

- Step Response Droop
  - 52 mV
  - Nearly 5%
  - Same as tolerance

\[ Z_{target} = \frac{V_{dd} \times \text{tolerance}}{I_{transient}} = \frac{1 \times 5\%}{1.55} = 32 \text{ mOhm} \]

\[ Z_0 = \sqrt{\frac{L}{C}} = \sqrt{\frac{50.7 \text{ pH}}{50 \text{ nF}}} = 32 \text{ mOhm} \]

To have step response droop = tolerance, make \( Z_0 = Z_{target} \)
Resonance Response – Switched Capacitor Load

- Estimate P-P noise
  - \( Z_{\text{peak}} \) is 103 mOhms
  - \( I_{\text{tran}} = 1.55A \) pulses for 5 nSec

\[
PP_{\text{resonance}} = \frac{4}{\pi} I_{\text{tran}} Z_{\text{peak}}
\]

\[
= \frac{4}{\pi} \times 1.55 \times 100 \text{m} \Omega
\]

\[
= 198 \text{m} \Omega
\]

- The \( 4/\pi \) comes from Fourier transform of square wave

- Actual P-P noise
  - 197 mV

- Mitigate resonant peak by
  - Reducing L
  - Increasing C
  - Increasing R (damping)
Compare Impulse, Anti-Impulse and Step Responses

- Anti-impulse is one missing pulse
  - Signature is nearly opposite that of impulse

- Compare droops
  - Impulse
    - 29 mV
  - Step
    - 55 mV
  - Anti-impulse
    - 36 mV

- Mitigation
  - Only C helps impulses
  - Both L and C help step response
Anti-step Response – Switched Capacitor Load

- **Anti-step happens when current goes away**
  - Signature is nearly opposite that of step response

- **Compare responses**
  - Step droop
    - 56 mV
  - Anti-step peak
    - 38 mV
    - Starting point is down because of DC IR drop

- **Step response should have more damping from on-die load**
  - Current source load does not show this
Summary

- PDNs are best analyzed and designed in the frequency Domain
  - Reactive components: R, L and C

- PDN time domain responses are all the only thing that matter to the product
  - Impulse, Step, Resonance responses must be managed

- The Target Impedance is the reference level to determine the performance of PDN
  - The step response will stay within tolerance if \( Z_0 = Z_{\text{target}} \)
  - The \( p-p \) resonance response is determined by \( Z_{\text{peak}} \)

- CMOS dynamic current comes from a series of current (charge) impulses
  - Logic activity draws an impulse of charge at each clock edge
  - Average clock cycle charge is calculated from bench current and frequency
  - On-die voltage droop from single impulse is calculated from \( Q=CV \)

- The on-die voltage must droop before current comes in from outside world
  - Capacitor \( \frac{dv}{dt} = \frac{I}{C} \)
  - Inductor \( \frac{di}{dt} = \frac{V}{L} \)
  - Large signal transient current is very important, small signal \( \frac{di}{dt} \) (slope) is not very important

- Switch capacitor loads behave like CMOS
  - Current source loads have no damping

- PDN time domain noise is mitigated by:
  - Capacitance for clock edge impulse response
  - Capacitance and inductance for step response
  - Resistance (q-factor) for resonance response

\[
Z_{\text{target}} = \frac{V_{\text{dd}} \times \text{tolerance}}{I_{\text{transient}}}
\]

\[
Z_0 = \sqrt{L/C}
\]

\[
Z_{\text{peak}} = X \cdot Q = \frac{X^2}{R} = \frac{L/C}{R}
\]

\[
Q_{\text{factor}} = \frac{Z_{\text{peak}}}{Z_0} = \frac{Z_0}{R_{\text{loop}}}
\]

\[
Q_{\text{cycle}} = \frac{I_{\text{dynamic}}}{f_{\text{clock}}}
\]

\[
V_{\text{droop}} = \frac{Q_{\text{cycle}}}{C} = \frac{I_{\text{dynamic}}}{f_{\text{clock}}} \cdot \frac{1}{ODC}
\]

\[
V_{\text{droop}} = I_{\text{step}} \times Z_0
\]

\[
PP_{\text{resonance}} = \frac{4}{\pi} I_{\text{transient}} Z_{\text{peak}}
\]
PDN Tutorial contents were drawn from these publications


BACKUP SLIDES

- Comparison of current source, current impulse and switched capacitor loads..
Impulse Response – Compare PWL Current and Switched Capacitor Load

- Impulse of charge is consumed from PDN
  \[ q = \frac{I_{\text{dynamic}}}{f_{\text{clock}}} \]

- Triangle current source
  - dotted
  - PWL current curve
  - Area under curve is charge consumed

- Switched Capacitor Load
  - Solid
  - Smooth current curve
  - Capacitor load calculated to consume correct charge

- Small amount of current (blue) comes in from inductor during current pulse
  - Slightly reduces voltage droop

\[ V_{\text{droop}} = \frac{I_{\text{dynamic}}}{f_{\text{clock}}} \frac{1.55\, \text{A}}{1\, \text{GHz}} \frac{50\, \text{nF}}{\text{ODC}} = 31\, \text{mV} \]
Impulse Response – Zoomed Out Compare

- Impulse of charge is consumed from PDN
  \[ q = \frac{I_{dynamic}}{f_{clock}} \]
- Triangle current source
  - PWL current curve
- Switched Capacitor Load
  - Smooth current curve
  - Capacitor load calculated to consume correct charge

\[ V_{drop} = \frac{I_{dynamic}}{f_{clock}} \frac{ODC}{50nF} = 1.55A/1GHz = 31mV \]
Step Response

- Straight current source
  - dashed

- Impulse current source
  - dotted

- Switched capacitor load
  - Solid

- Currents
  - Load current is green
  - Bump current is blue

- Voltages are similar
  - Charge and time averaged current consumed from on-die capacitance is similar
Resonance Response

- Straight current source

- Impulse current source

- Switched capacitor load

- Currents
  - Load current is green
  - Bump current is blue

- Voltages are similar
  - Charge and time averaged current consumed from on-die capacitance is similar
Resonance Response – triple the current

- More voltage droop at higher current levels
  - Baseline current has tripled
  - $Z_0$ is now 3x $Z_{\text{target}}$
- Sources behave differently
  - Current sources draw same current without regard to voltage
  - Switched capacitor circuit draws less current at less voltage
    - Has more damping