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MLC Capacitor Parameters for Accurate Simulation Model

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Abstract

Low impedance power distribution systems (PDS) must be designed by CAD tools to insure that a low and flat target impedance (i.e. 1 mOhm) is met over a wide frequency range. Accurate models for Multilayer Ceramic (MLC) capacitors are required for simulation. Traditional resistance, inductance and capacitance (RLC) models do not exhibit the frequency dependent effects that are observed when the capacitors are mounted on a low inductance PCB or test fixture. A transmission line model for the capacitors gives more accurate simulation results. Model parameters are extracted from S21 measurements of the capacitor mounted on a low inductance fixture.

Introduction

Today's power distribution systems for computer applications are often required to meet a 1 mOhm target impedance. This is driven by the need to supply 100 watts or more at about 1V to micro processors, memory and communication chip sets. CAD systems are used to design low target impedance PDSs in order to insure that a flat impedance is met over a wide frequency range [1]. Accurate analysis of the PDS requires accurate simulation models for the major PDS components. The traditional series RLC model is often used to simulate MLC capacitors but it does not exhibit the frequency dependent effects that are observed with hardware measurements. A more sophisticated simulation model is required [2, 3, 4, 5]. MLC capacitors used for decoupling or bypass in applications in computer systems are usually mounted on low inductance pads connected to power planes that provide a low impedance environment. Measurement techniques that produce accurate data for extraction of capacitor model parameters are needed.

Traditional model inaccuracies

The impedance vs frequency of a measured 1uF X5R 0603 size capacitor is shown in Figure 1. Also shown is a simulated series RLC model for the capacitor with parameters chosen for the best fit match. At frequencies below series resonance, capacitance value (*Cap*) is the dominant parameter. The impedance minimum at series resonance is determined by the equivalent series resistance (*ESR*) value. The frequency of the minimum is determined by the inductance and capacitance according to the formula

$$f_0 = \frac{1}{2\pi\sqrt{ESL \cdot Cap}} \tag{1}$$

where *ESL* is the equivalent series inductance. But after choosing *Cap, ESR* and *ESL* for the best match at low frequency and at series resonance, there is a poor match at higher frequency. This is because *ESL* and *ESR* at frequencies above series resonance are a function of frequency. The frequency dependent effect is observed when the capacitor is mounted in a low inductance fixture such that the internal inductance of the capacitor is not dominated by the inductance of the mount.

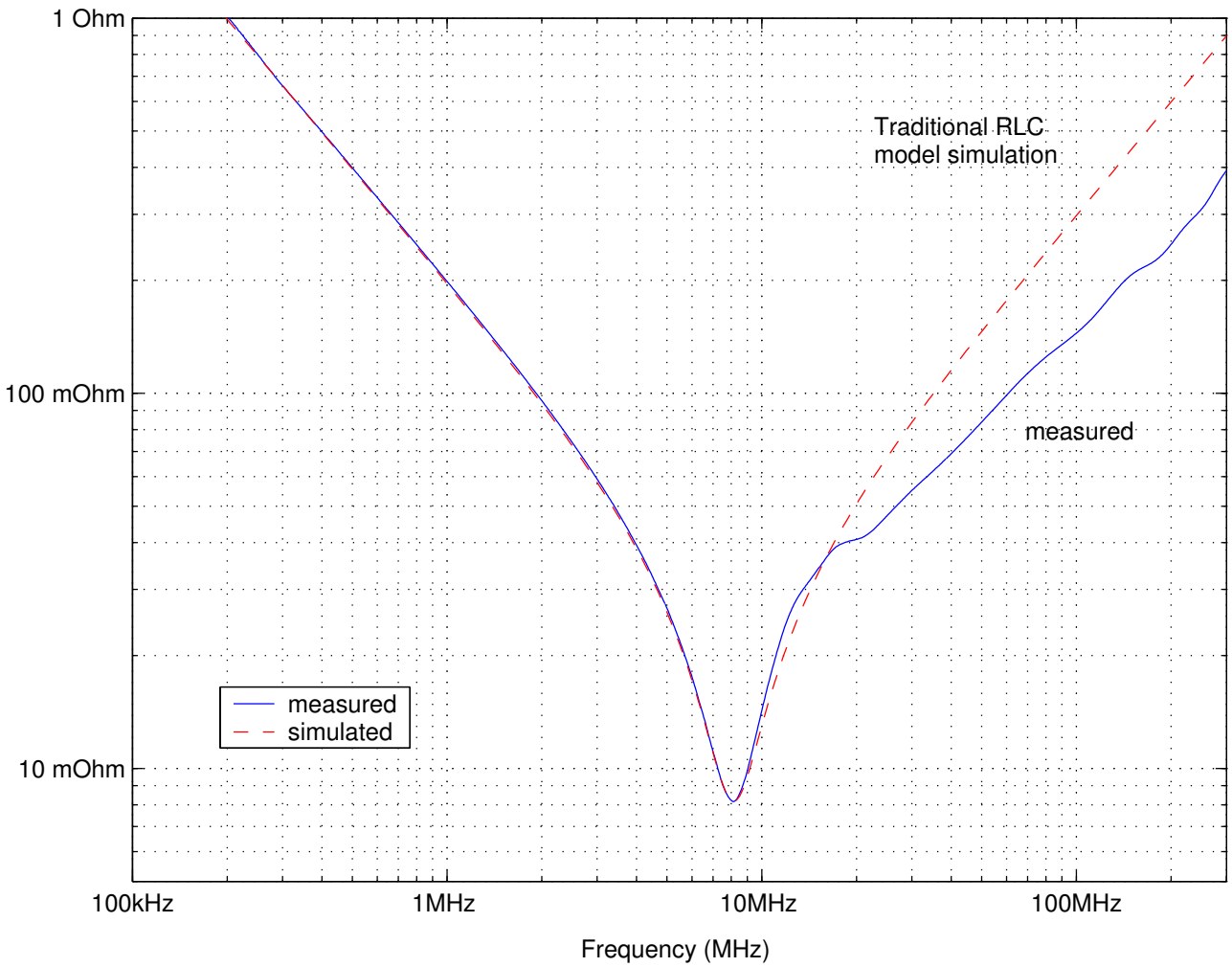

Figure 1: Measured and simulated results for 1 uF 0603 MLC capacitor. A series RLC model is simulated with R=8.2 mOhms, L=746 pH and C=801 nF. The traditional model gives poor matching above series resonance.

The low inductance pads on low impedance power planes in computer PDS applications provide such an environment. From a computer product perspective, a low inductance mount is highly desirable because it extends the effective range of the capacitor to higher frequency and fewer capacitors are required to accomplish the same decoupling performance. It is important to measure and model capacitors in an environment similar to their use conditions in order to gather model parameters that will be used for PDS simulation. A sufficiently accurate model will be able to capture the frequency dependent nature of *ESR* and *ESL* in a way that the simple series RLC model cannot.

Capacitor construction

The construction of an MLC capacitor, which is the basis for a more accurate model is schematically shown in Figure 2, together with the top power plane layers of a printed circuit board (PCB). The diagram is almost to scale in that the thickness between the PCB power planes and the distance between the top power plane and the capacitor is much less than the height of the capacitor. These PCB design features minimize the mounting inductance and are important for extending the frequency range where the capacitor is effective for decoupling applications. There is often a ceramic filler plate or coating [5]

in the bottom of the capacitor that is used to make the height of consistent with capacitors of the same body size but different capacitance values. The filler plate may be a large contributor to the intrinsic inductance of the capacitor.

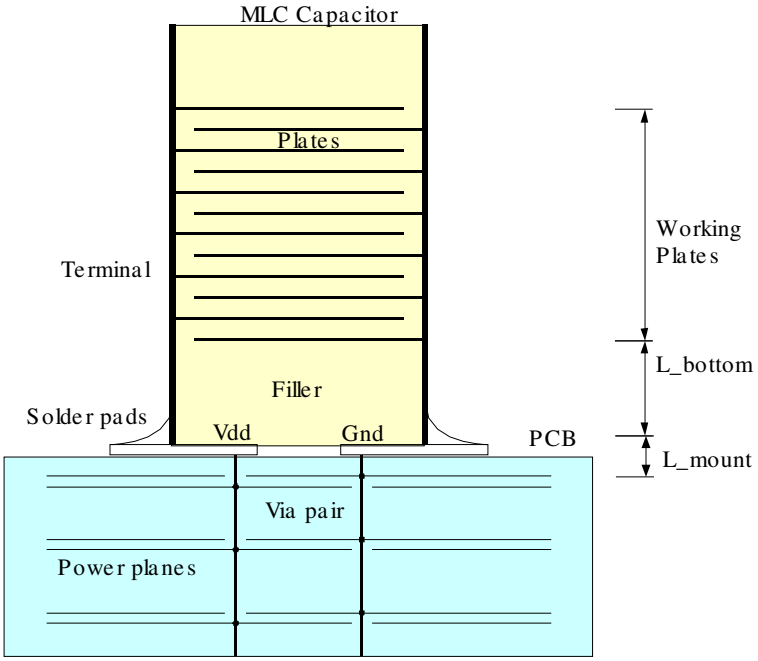

Figure 2: Construction of MLC capacitor mounted on PCB fixture. Inductance is associated with the working plates, the filler plate and the mount.

Further up and away from the PCB power planes is the working portion of the capacitor where many conductive and dielectric plates are stacked up for the purpose of charge storage. The number and thickness of the ceramic plates and the effective dielectric constant determines capacitance value. The number, thickness and conductivity of the conductive layers are the dominant factors that determine the *ESR* of the capacitor. The capacitance and *ESR* are primarily determined within the working plate region of the capacitor.

Inductance however is a function of the path or loop that the current takes as it makes it's way from the PCB power plane to ground plane. Inductance is associated with the magnetic field which is concentrated inside the loop where current flows. It is increased by increasing the loop dimensions and decreased by minimizing the area of the loop. Important dimensions in this loop include the horizontal distance between PCB vias and mounting pads and the length of the capacitor between terminals. The important vertical dimensions include the distance between PCB power planes, via height to the surface of the PCB, solder pads and terminal geometries, the thickness of the capacitor filler plate, and the height of the working plates within the capacitor. Capacitor values near the maximum capacitance for a given body size tend to be completely full of working plates whereas capacitors of lesser value may have a larger filler plate and have their working plates concentrated near the center of the body. Lesser valued capacitors may also have thicker dielectric plates of the same dielectric constant material.

The ESL of the capacitor is therefore determined not only by the dimensions of the working plates but also by the dimensions of the filler plate, mounting structures and PCB vias and power planes. The inductance discussion is complicated by the concepts of self inductance, partial inductance, mutual inductance and interactions of magnetic fields throughout the entire PCB and capacitor structure. The ESL as defined in equation (1) above is the equivalent series inductance that is a property of the entire

loop of the current path. The entire loop must be considered in any PDS simulation. Measurement of capacitor parameters to be used in simulation requires the inductance of the fixture to be backed out so that the parameters are not highly influenced by the inductance of the fixture. The inductance of the PCB mounting structure must be quantified and added back into simulations of the PDS in order to achieve accurate results.

Capacitor model

A transmission line circuit model has been proposed that mimics the construction of MLC capacitors and mounting structures as discussed in the previous section. The topology of the model is shown in Figure 3. The capacitance of the working plates is represented by capacitors that are effectively in parallel at low frequency (C_p). The *ESR* is mostly in the conductive plates and is represented by the resistors (R_p) which are also effectively in parallel at low frequency. Because of the many thin ceramic dielectrics and relatively wide dimensions of the conductive plates, the inductance associated with the horizontal plates is very small.

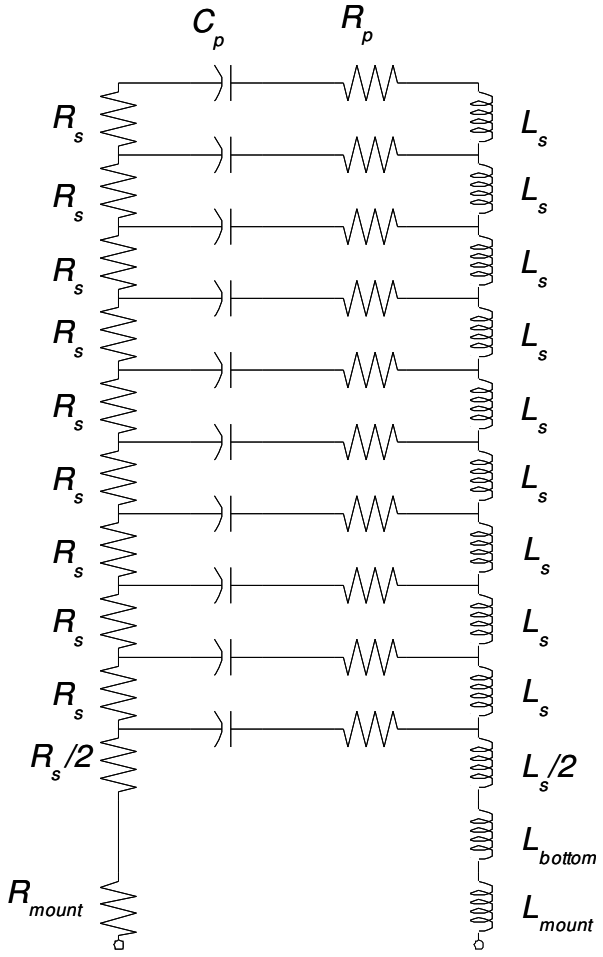

Figure 3: Transmission line circuit model for MLC capacitor.

The dominant inductance of the capacitor is associated with the vertical dimensions and mount. L_{bottom} is the inductance assigned to the portion of the loop near the filler plate. The loop area is further increased as current proceeds up the terminals past the working plates of the capacitor. These vertical inductances are in series and are designated L_s. The comparable series resistance is designated R_s. The frequency dependent nature of the capacitor can be envisioned by considering the relationship between the vertical and horizontal components of this model. At low frequency below series resonance, the relatively high reactance of the capacitance $1/(j\omega C)$ dominates over the reactance of the series inductance $j\omega L$.

At high frequency (above series resonance) the impedance roles of the inductance and capacitance reverse. The relatively high reactance of the L_s inductors dominates and impedes current from reaching the capacitance that is higher up the ladder. The effective inductance of the capacitor is diminished. At high frequency there are effectively fewer R_p resistors in parallel so the *ESR* of the capacitor increases above series resonance. This is a qualitative explanation for frequency dependent nature of capacitors on low inductance mounts. This phenomenon can only be observed when the fixture plus filler plate inductance (L_{mount} + L_{bottom}) is less or much less than the intrinsic inductance of the capacitor which is associated with the working plates (sum of L_s).

At series resonance, the vertical inductors and horizontal capacitors behave like a ¼ wavelength lossy transmission line with the high impedance open circuit at the end appearing to be a low impedance at the PCB pads. This property enables the calculation of the circuit parameters shown in Figure 3 [6].

Model to hardware correlation

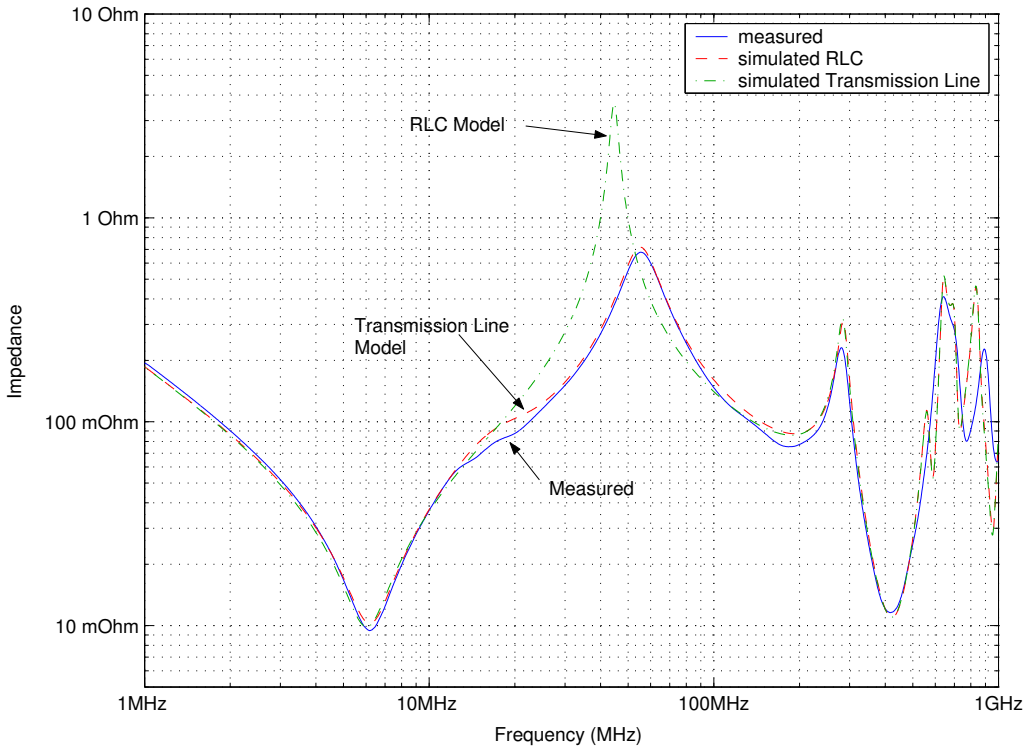

Figure 4: 1 uF capacitor mounted on PCB. Measured impedance and simulated results of the RLC and transmission line models are shown.

Figure 4 shows the measured impedance vs frequency for the 1 uF capacitor of Figure 1 mounted on PCB power planes with a low inductance mount. Also shown in the figure is the simulated results of the series RLC capacitor model and the transmission line capacitor model. Both capacitor models correctly

predict the impedance minimum at about 6 MHz associated with series resonance but at higher frequency the two simulations diverge. The peak at about 60MHz is due to the inductance of the mounted capacitor in parallel resonance with the capacitance of the PCB power planes.

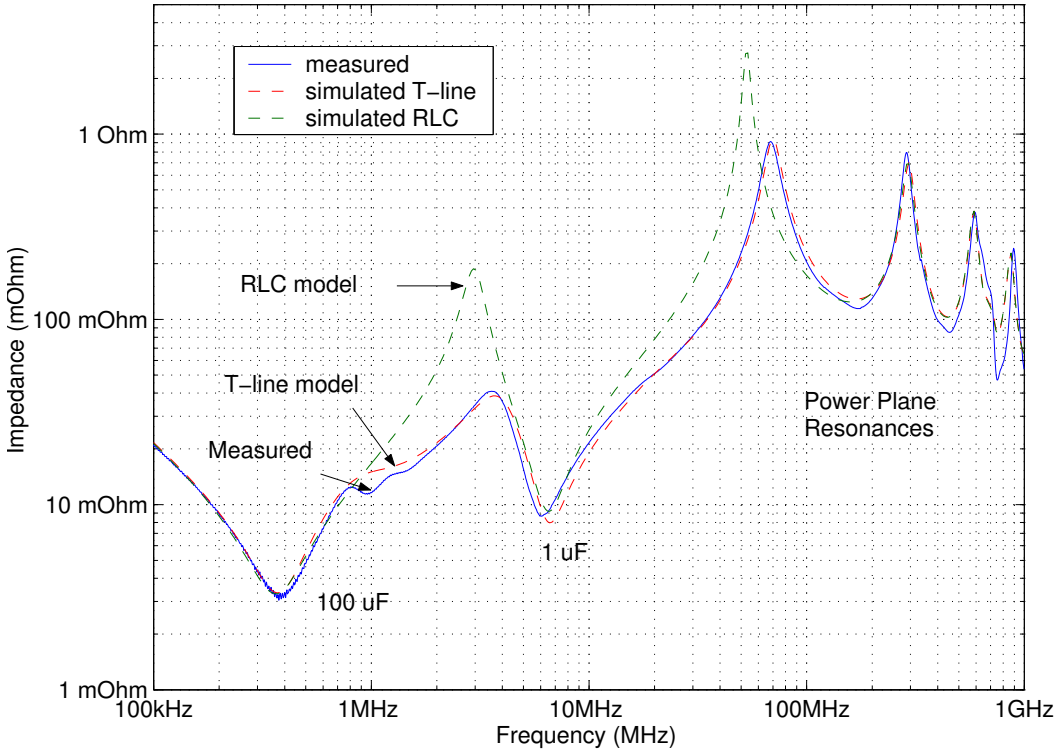

Figure 5: A 1uF and a 100 uF capacitor mounted on PCB. Measured and simulated results are shown.

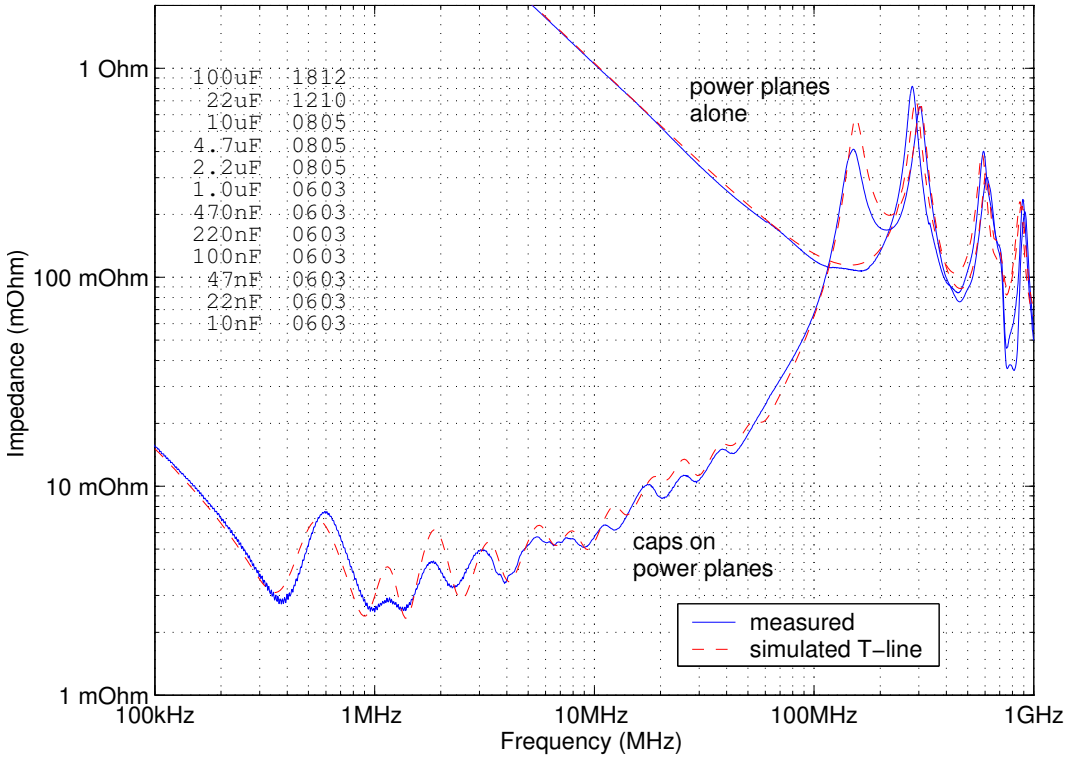

Figure 6: A dozen capacitor values mounted on PCB.

The transmission line capacitor model correctly predicts this resonant peak better than the traditional series RLC model because of the reduction of *ESL* and increase in *ESR* of the mounted capacitor at frequencies above series resonance. The power plane impedance, including cavity resonance effects, have been modeled according to the techniques described in [7].

Figure 5 compares the measurement of two capacitors mounted on power planes to simulation results for RLC and transmission line capacitor models. Once again, the resonant peaks are predicted better by the transmission line capacitor model because of the frequency dependent effects. Figure 6 shows the measured and simulated curves for a dozen capacitors mounted on power planes. As more capacitors of different values are added, it is possible to meet a target impedance less than 1 mOhm up to 50 Mhz or more. The most accurate results come from the more complex capacitor models. Careful capacitor measurements must be made to develop the parameters for such models.

Measurement of Transmission Line Parameters for Capacitor Model

As mentioned above, capacitors must be measured on very low inductance fixtures in order to observe the frequency dependent nature of *ESL* and *ESR*. The inductance of the fixture should ideally be much less than the intrinsic inductance of the capacitor. A VNA is used to measure the S21 parameters of the capacitors in a way similar to that described in [8]. Port 1 forces current from essentially a 50 Ohm current source into the capacitor. Port 2 measures the voltage at some point along the current path from port 1. The measured S21 data is easily converted to impedance. Three data points are required along the impedance vs frequency curve to determine the parameters of Figure 3.

1- a point one decade below series resonance determines the capacitance
2 - a point at the series resonance minimum determines *ESR* and *ESL*
3 - a point a decade above series resonance determines the high frequency L.

A fourth point is required to obtain the fixture inductance. This is the same measurement but the capacitor is replaced with a shorting bar that has dimensions similar to that of the capacitor DUT. Figure 7 shows the measurement of a 1 uF capacitor and shorting bar.

Fixture

The fixture used to measure the data in Figure 7 is shown in Figure 8, with and without a capacitor mounted. Figure 9 shows the full size of the fixture. This simple fixture is a pair of 50 Ohm coaxial cables with SMA connectors for the VNA. The DUT capacitor is soldered across the continuous 50 Ohm transmission line as shown in Figure 10. A “through” calibration is performed before attaching the DUT. The port 1 transmission line is the current source and the port 2 transmission line senses the voltage at the DUT. A shorting bar soldered into the DUT position gives S21 data for the shorted fixture that is consistent with 83pH inductance. Other fixtures have been tried but it is difficult to achieve inductances below 100pH. This fixture however may not be appropriate for a measurements in a production environment. Further work is required to develop fixtures that are sufficiently low in inductance to exhibit the frequency dependent nature of capacitors and also be consistent with the manufacturing environment. Details concerning the extraction of capacitor parameters from the 3 measured data points on the capacitor impedance profile together with the fixture inductance are given in [7]

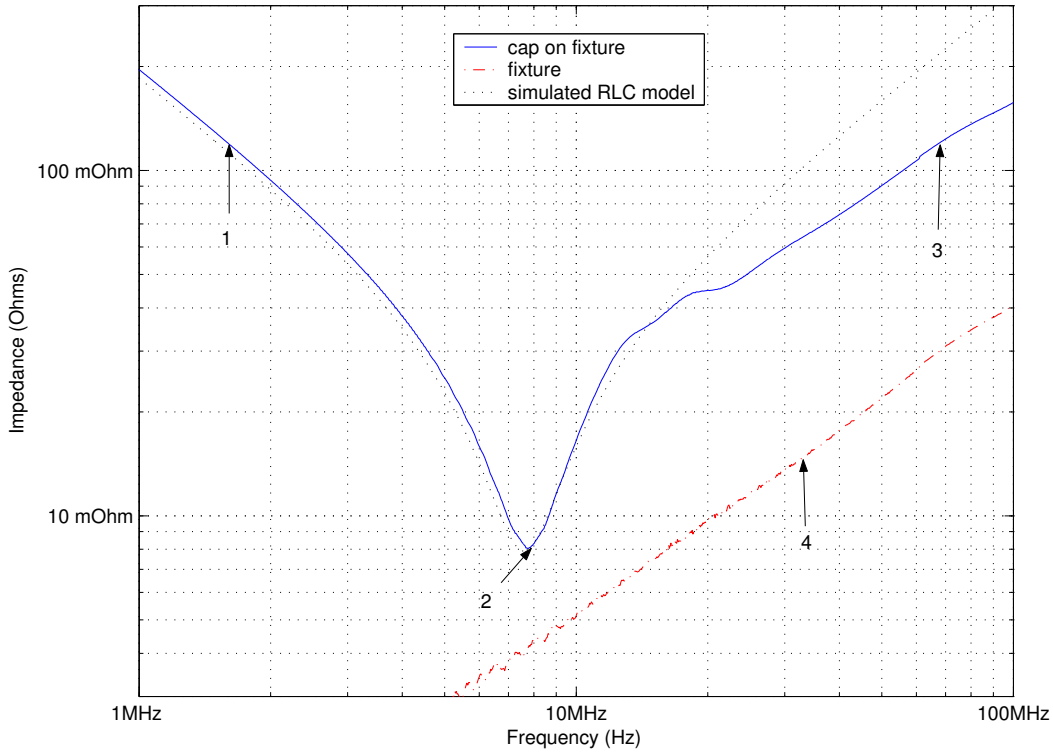

Figure 7: Measurement results for 1 uF capacitor and shorted fixture. Four data points are required to determine the parameters for Figure 3.

Figure 8: Low inductance measurement fixtures without (top) and with (bottom) a capacitor mounted as the DUT.

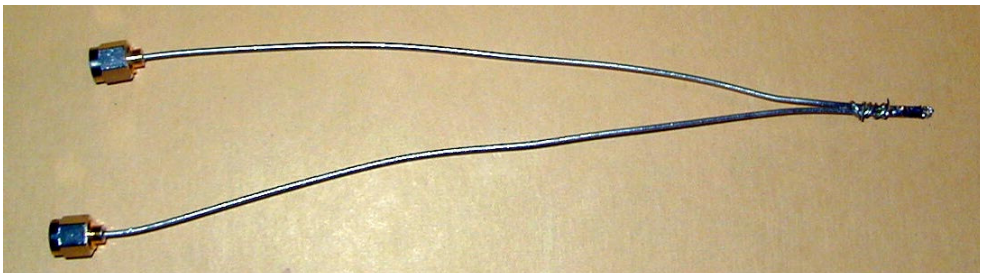

Figure 9: Low inductance wire fixture used to measure MLC capacitors.

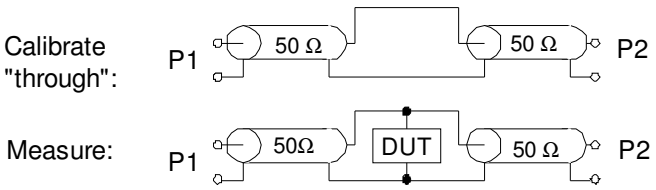

Figure 10: Schematic diagram of the calibration and measurement of the device under test (DUT, capacitor).

Conclusion

A transmission line model which is more accurate than the traditional RLC model has been developed for MLC capacitors. Simulation results correlates well with hardware measurements of multiple capacitors mounted on low inductance PCBs. Model parameters are gathered from S21 measurements of capacitors mounted on low inductance fixtures. The fixture inductance must be known so it can be backed out of the capacitor measurements. Further work is required to develop low inductance fixtures suitable for a manufacturing test environment.

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