System Power Distribution Network Theory and Performance with Various Noise Current Stimuli Including Impacts on Chip Level Timing

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***Abstract*-Power Quality has become a determining factor in product performance and reliability. The reactive portions of the power distribution network (PDN) have a greater effect on power quality than DC IR drop. Resonance in the parallel inductance and capacitance network creates an impedance peak in the frequency domain and undesirable voltage noise in the time domain. The on-chip voltage noise is usually much higher than PCB PDN noise. A method of determining and simulating circuit parameters and comparing results to a target impedance is presented. A test vehicle has been built and measured to provide laboratory measured results for PDN voltage noise. Switching current patterns are defined which generate typical and pathological voltage waveforms. PRBS patterns are used as a characterization technique to provide reasonable worst case resonance stimulation. The voltage noise is responsible for measured timing and jitter degradation in logic circuits.**

I. Introduction

Power distribution is an important part of the infrastructure necessary to run all types of silicon products but it is often neglected during the design process. The power quality may limit the performance of circuits and often determines how reliably they work. Much has been written about PDN at the printed circuit board (PCB) level [1] including voltage regulation and decoupling. To really address the power distribution issue, the entire system must be considered including the chip, package and PCB.

Chip designers often consider DC voltage drop, but system reactances including chip capacitance and the inductance of the package and PCB structures usually dominate over IR drop[2]. The reactances form resonant structures that store and release energy in certain frequency bands. PDN resonances are a property of the system. It is not possible to predict the resonances by looking at the chip, package or PCB individually. The entire system must be considered in order to predict the resonant impedance peaks in the frequency domain and the minimum and maximum voltages seen by the on-chip circuits in the time domain.

In the present state of the industry, large companies have developed tools and methodologies to consider the entire power distribution system [3]. These techniques are often complex and involve electromagnetic (EM) solvers operating on large data bases for the chip, package and PCB structures. EM software companies such as Sigrity [4] have developed rigorous analysis packages to deliver accurate system models, usually in S parameter format. Apache [5] has gone one step further to combine chip parameters along with the package and PCB parameters to predict the quality of the on-chip power. In most cases, fairly mature designs with artwork databases are required in order to do the analysis.

In this paper, the authors will give a qualitative description of the PDN resonance phenomenon including the chip, package and PCB parameters that are most responsible for causing it. We will quantify the important inductive, capacitive and resistive parameters seen in typical systems. Simulation of these parameters will show the typical resonant impedance peaks and resulting time domain power waveforms that must be tolerated by the circuits. We will show measured on-chip voltage and model to hardware correlation. Three fundamental stimuli are developed to systematically characterize and understand the on-chip PDN properties and voltage noise. Finally, we will show the circuit performance implications of PDN noise.

II. Power Distribution Network Theory

The starting point for PDN design is with the target impedance [6]. It is a simple ohms law calculation that gives a good indication of how much chip and packaging resource (on-chip capacitance, on-package capacitance, number of pins, vias, size of power planes, etc.) is needed in order to deliver power to the circuits on-chip with reasonable quality.

Figure 1 shows an ideal voltage source connected to a circuit load through an impedance. The current drawn by the load is rarely constant but changes with time according to the present operation of circuits. On a long time scale, the current load will change depending on whether the chip is in a power savings mode, an idle state or busily processing data. These power transients will cause voltage variations at the load when the current passes through the impedance.

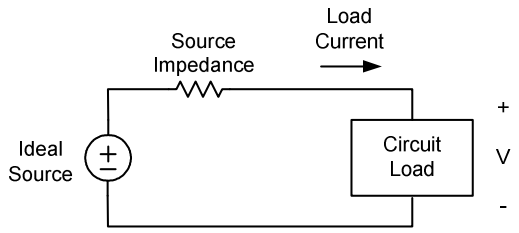

Figure 1. Circuit load on-chip that is connected to an ideal voltage source through some source impedance. Changes in load current produce a change in the power supply voltage seen at the circuit terminals.

To help formulate design guidelines for PDN design, a target impedance is established that is sufficiently low to deliver high quality power at the least possible cost. It is a target because if the actual impedance exceeds the target

impedance then circuits are in danger of malfunction. If the actual impedance is below the target impedance, it probably cost more than necessary. The target impedance is defined as

$$Z_{\text{target}} = \frac{Vdd \times tolerance}{I_{max} - I_{min}} = \frac{1.0\,V \times 0.05}{7A - 2A} = 10\,mOhm \quad (1)$$

For example, the circuits on a power supply that is nominally 1.0 Volts may be able to tolerate 5% changes in the power supply voltage without performance degradation. During normal operation, user activity may cause a maximum of 7 amps to be consumed, or at some time later, a minimum of just 2 amps during idle or power savings modes. The transient current is the maximum minus the minimum current, 5A for this example.

At this point, it is useful to discuss the nature of inductive and capacitive reactive components in both series and parallel configurations. Figure 2 shows a schematic diagram for 3 components connected in series and parallel configurations: 100nF, 4mOhms and 120pH. From the outside world (package pins) the components are in series, but from the silicon circuits perspective the on-chip capacitance is in parallel with the package inductance. With a vector network analyzer (VNA) it is possible to measure the series circuit to determine the reactive parameters (R, L and C) that are inside the package [7]. When the silicon circuits are functioning in a system, the parallel schematic for the same components represents their connection topology.

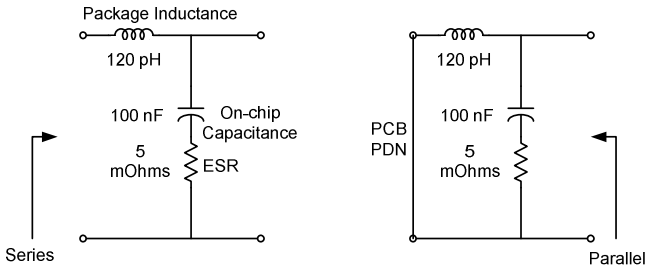

Figure 2: Series and parallel circuits for the RLC component values which represent the lumped elements for a core logic PDN. The circuits on-chip see the parallel circuit when the packaged silicon is attached to a low impedance PCB PDN.

Figure 3 shows simulation of the series and parallel circuits. In each case the impedance of the inductor is jwL and the impedance of the capacitor is $1/(j\omega C)$. The series circuit gives a dip in impedance and the parallel circuit gives a peak in impedance. The role of the resistance (equivalent series resistance, ESR) is to define the minimum impedance value for the series circuit and determine the maximum peak for the parallel circuit. The resonant frequency is always $f_0 = 1/(2\pi\sqrt{LC})$. The Q-factor, defined as the reactive impedance divided by the resistive impedance at resonance, is $Q = X/R = \sqrt{L/C}/R$. The height of the peak in the parallel resonance is approximately $XQ = X^2/R = (L/C)/R$.

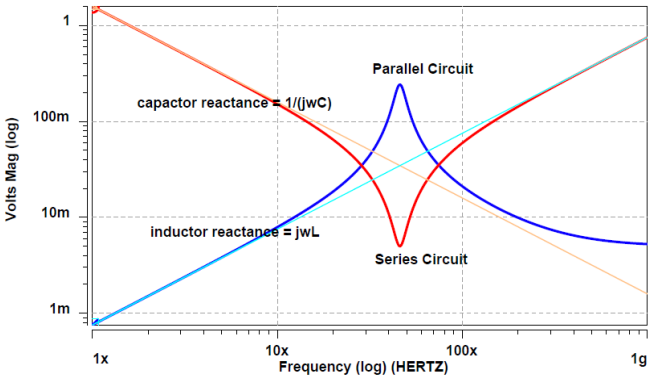

Figure 3: Simulation of series and parallel circuits of Figure 2. The ESR controls the Q-factor, the depth of the dip and the height of the peak.

III. Typical PDN for Core Power

A real life PDN has capacitive and inductive reactances which result in a non-trivial impedance for practical applications. Figure 4 shows a schematic diagram with several components of a power distribution system. The frequency domain impedance of this system is also shown with frequency on a log scale from the kHz to the GHz range. The actual impedance should be compared to the flat target impedance. It is possible for user activity to stimulate the PDN at any clock sub-rate so it is desirable to choose components that meet the flat target impedance. The impedance is dominated by certain circuit parameters in different frequency bands. The components are located approximately below the frequency bands that they control. The most prominent impedance peak is at 43 MHz and is due to the on-chip capacitance resonating with the PCB mounted package inductance and is known as chip/package resonance.

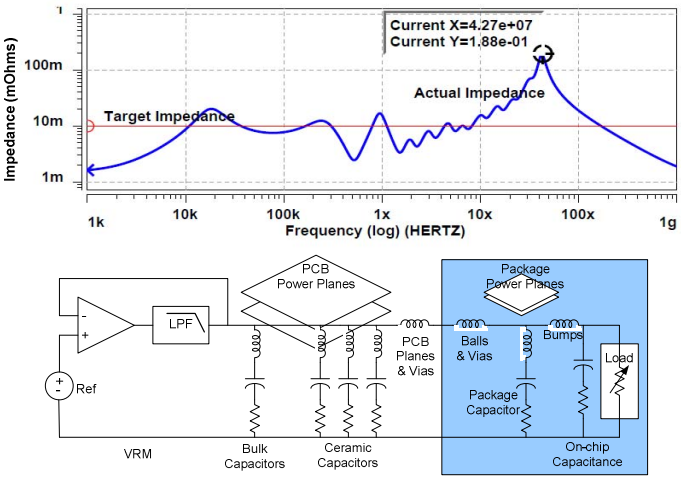

Figure 4: The PDN is made from components that control the impedance in different frequency bands. An impedance profile of a typical core logic PDN is shown above with a peak at about 43 MHz which far exceeds the target impedance.

Figure 5 shows time domain simulation results for the same PDN circuit. The load draws fast transient currents consistent with the target impedance calculations above. The power transients are fast, occurring with just several nSec rise

time. Typical power transients can occur in just a few clock cycles and have high frequency content according to the rise time of the step function. Any frequency peak below about 300MHz will be stimulated. In this simulation, the frequency peak at 43 MHz results in a damped sinusoid at that frequency. Note that there is a negative-going sinusoid with the increasing power transient and a positive-going sinusoid with decreasing power transient.

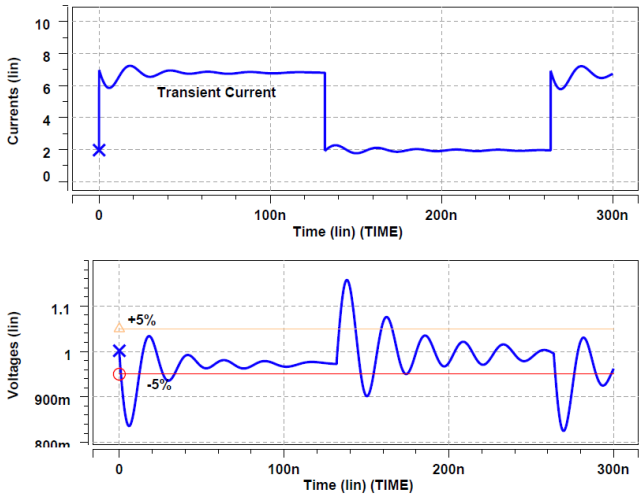

Figure 5: The on-chip load draws a 5 amp time domain transient from the PDN. The on-chip voltage has dips and peaks associated with the current transients and rings out in a damped sinusoid at the PDN resonant frequency.

A Resistive load has been chosen to represent the CMOS circuitry rather than a constant current source. CMOS circuitry draws more current as the power supply voltage is increased and less current when the power supply voltage is decreased, very similar to a resistor. A constant current source does not give the proper response to variations in power supply voltage nor does it give the proper damping. Therefore, a time varying resistor is chosen for the PDN load leading to the non-square current waveforms and power transients.

The increasing and decreasing power transients were spaced out in time so that they did not overlap and it is possible to see the affect of each. But user activity can stimulate the PDN at any random frequency that is a sub-rate of the clock. Figure 6 shows simulation of the same circuit where the pathological aggressor frequency has been chosen. The power transients occur at exactly the resonant peak frequency of 43 MHz. Damped sinusoids superimpose on top of one another and the waveform builds up over several cycles. With a nominal power supply voltage of 1.0 volts, maximum and minimum voltage excursions of 1.39 and 0.59 volts are simulated for an actual power supply tolerance of +-40%. This has happened because the actual impedance greatly exceeded the target impedance.

An interesting aspect of the parallel resonant circuit is the magnetic energy in the inductor transferring to the electric field of the capacitor. Figure 6 shows both the electric potential across the capacitor during resonance and the current flowing through the inductance which is responsible for magnetic energy. It is a surprise to many that with an average current of 4.5 amps, there are periods of time where 14 amps flow into the chip and other periods of time where 7 amps flow out of the chip.

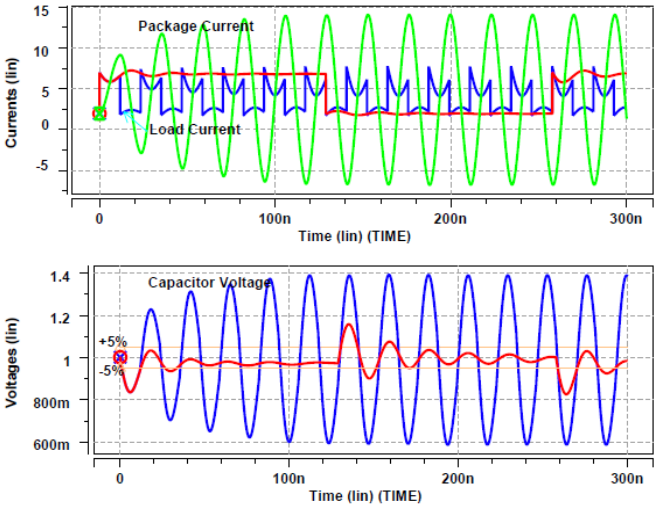

Figure 6: User activity creates power transients that cause the PDN to be stimulated at the resonant frequency. Because the target impedance was exceeded, waveforms superimpose on one another and build up to far exceed the power supply tolerance limits.

The peak in the parallel resonance circuit is what causes PDN trouble. From the equations above, it is evident that the Q-factor determines the height of the resonant peak. Resistance is desirable and always provides damping for the parallel resonant circuit. Increasing inductance always increases the Q-factor and increasing capacitance always decreases the Q-factor. Unfortunately, increased on-chip capacitance and decreased package inductance is always more expensive. As anticipated, the cost and performance of the PDN are highly related.

IV. Physical Structure and Circuit Parameter

Figure 7 shows a cross section of the structure of a physical system. Almost all of the capacitance for the resonant structure is on the chip. On a well bypassed board, PCB decoupling capacitors form a low AC impedance that is for practical purposes a short circuit. The chip is connected to the package with C4 solder bumps and the package is connected to the PCB with solder balls. Internal to both the package and the PCB are vias and power planes. Current travels in a loop from the PCB capacitors through the power plane, balls, vias and bumps and returns on a similar path on ground structures. This big loop has a loop inductance.

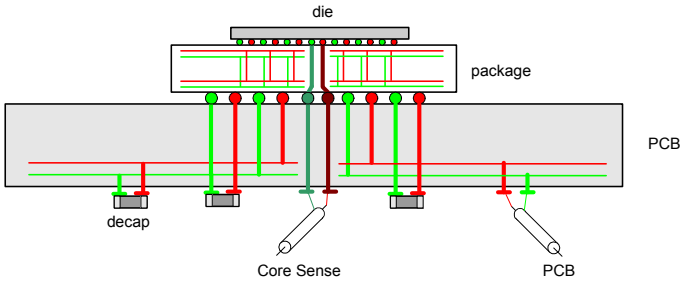

Figure 7: Cross Section of chip mounted on package and PCB. A current loop from the PCB decoupling capacitors is formed by the PCB power planes, vias, solder balls, package vias and chip solder bumps. Each portion of this loop contributes inductance which is active during chip/package resonance.

The most accurate way to obtain the loop inductance is with an electromagnetic simulator operating on the artwork databases for the chip, package and PCB. This is a large scale problem that is difficult to solve all at once and it is usually broken up into pieces to in order to fit into reasonable computer resource and simulation time. If a little less accuracy can be accepted, a spread sheet and simple electromagnetic approximations can be used to calculate the inductance of each piece of the system. The top level page of such a PDN resonance calculator spread sheet is shown in table 1. The circuit parameters that were simulated in figures 3, 4, 5 and 6 came from this calculator. The major sections of the table include calculation of the target impedance, system parameters such as on-chip capacitance and ESR, package inductance and resistance, and PCB inductance and resistance. The inductive and resistive parameters are summed up and treated as a parallel RLC circuit. The equations described above are used to calculate the resonant frequency and impedance peak. The ratio of impedance to target impedance is the figure of merit that should used to evaluate the quality of the PDN.

Table 1: PDN Resonance Calculator Spread Sheet.

Supply	**Vcc**	**Units**
Voltage	1.0	volts
AC Tolerance	5	%
Average Dynamic Current	10.0	amps
transient (% of dynamic)	50	%
AC Target impedance	10.0	mOhms
On-chip Capacitance	100	nF
On-chip Capacitance ESR	1.0	mOhm
number of Vcc/Vss ball pairs	39	
Package Inductance	20	pH
Package resistance @ resonance	0.944	mOhm
PCB via length	121	mils
PCB via inductance	50	pH
PCB plane dielectric thickness	6	mils
PCB plane squares	0.27	
PCB plane inductance	50	pH
PCB resistance @ resonance	2.31	mOhm
Total inductance	120	
Total resistance at resonance	4	
Resonant frequency	46	MHz
Resonant peak	281	mOhm
Ratio (Z to Z_target)	28	
Q-Factor	8.1	

V. On-Chip PDN Noise Measurements

To monitor the real time on-chip voltage noise, a high bandwidth probe is implemented on one instrumental test chip. As shown in Figure 7, a pair of package balls is connected to on-chip power and ground metal network directly through package plated-through-hole (PTH) vias and chip bumps. This on-chip sensing probe is isolated from rest of power and ground network in package and PCB. The impedance of the probe in package and chip are well controlled, and the bandwidth is beyond 1GHz. The on-chip voltage noise is measured through this specially designed on-chip sensing probe.

Figure 8 shows a scope shot of one on-chip PDN voltage noise waveform as well as PCB level of PDN noise. A large number (~100,000) of T Flip-Flops (TFF) are implemented on the test chip which are triggered once. The first on-chip voltage drop is due to the synchronized switching current drawn by the TFFs. The voltage sag is 105 mV out of 1.1V nominal voltage rail. The falling edge of the voltage sag is less than 500ps. For such a fast switching event, all currents must be drawn from on-chip capacitance due to its physical proximity and low inductance. After the sudden voltage sag, PCB PDN starts to provide charge to replenish the on-chip capacitance through the package and PCB inductance.

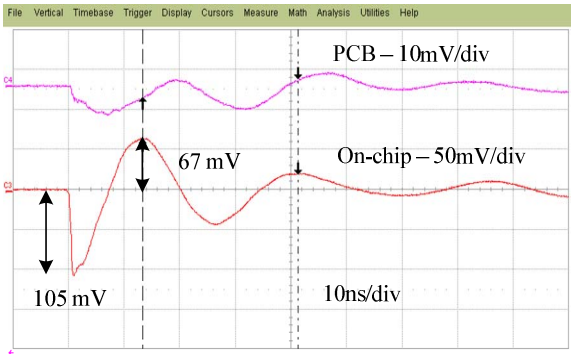

Figure 8. Measured on-chip and PCB voltage noise with one switching event.

The following peak is the inductive overshoot, which is 67mV. The damped voltage resonance is determined by the system PDN resonance frequency and Q-factor. The on-chip pk-pk voltage noise is 172mV, which is 16% of 1.1V nominal voltage rail. However, the pk-pk voltage noise on PCB is only 11mV, which is only 1% of 1.1V. This experiment shows that even though PDN noise at PCB level is well controlled, the chip-level PDN noise could be much higher. Circuit designers have to take this large on-chip voltage fluctuation into account when they design the on-chip PDN.

VI. Model to Hardware Correlation

On-chip PDN voltage noise is driven by the chip current drawn. To understand the nature of on-chip voltage noise, three important current terms are defined below:

1. clock edge current
2. charge per clock cycle
3. dynamic current.

Figure 9 illustrates the concepts of three current terms. The clock edge current is defined as an instantaneous on-chip current drawn by the switching logic at the clock rising edge (or falling edge). The clock edge current consists of a fast rising edge and an exponential falling edge. The fast rise time and fall time of the edge will vary according the nature of on-chip circuitry.

The probability density function (PDF) of the gamma distribution is chosen to represent the on-chip current drawn due to the waveform nature and the flexibility of adjusting rise and fall time. Synchronous digital logic behavior typically consists of a large number of non-critical paths that finish shortly after the arrival of the clock edge with a decreasing number of paths continuing to draw current as time progresses. The equation defining the PDF of a gamma-distributed random variable x is

$$f(x;k,\theta) = x^{k-1}\frac{e^{-x/\theta}}{\theta^k\,\Gamma(k)} \text{ for } x > 0 \text{ and } k,\theta > 0. \quad (2)$$

By adjusting two parameters with scale θ and shape k, a variety waveforms with different combinations of rise and fall time can be easily generated to mimic on-chip current drawn with different types of circuitry.

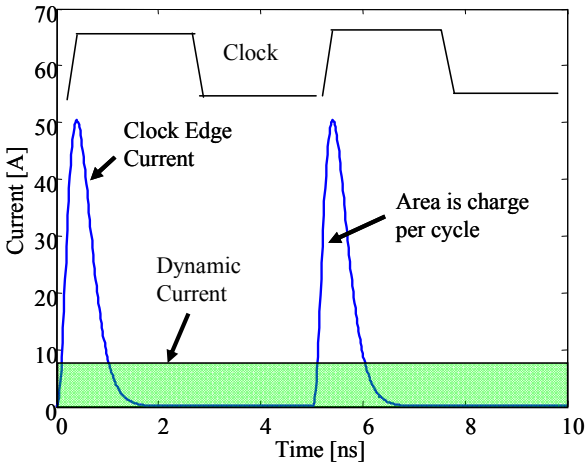

Figure 9. Schematic representation of on-chip current definition

The charge per clock cycle is defined as the charge consumed by the circuit in one clock cycle, which equals the integration of the clock edge current over one clock cycle.

$$Q = \int_0^T i(t)\cdot dt \quad (3)$$

The dynamic current is defined as time averaged current of clock edge current, and it can be calculated as

$$I_{dynamic} = Q/T = \frac{1}{T}\int_0^T i(t)\cdot dt \quad (4)$$

The dynamic current is proportional to the clock frequency; however, the charge per clock cycle remains constant over frequency.

A current controlled resistor model is developed to accurately model the on-chip circuit current load. The current profile is represented with a PDF of the Gamma distribution as discussed above. For the TFF circuitry implemented on the test chip, the rise time and fall time of clock edge current is 400ps and 900ps, which are extracted from circuit timing analysis and validated through model to hardware measurement correlation. Figure shows the simulation results. Table 2 summarizes the major parameters of the measurement and simulation results in terms of voltage sag, pk-pk amplitude and PDN resonant frequency. The difference between the measurements and simulation results are within a few percent. With the proposed chip load model, a good correlation has been achieved between the hardware measurement and simulations.

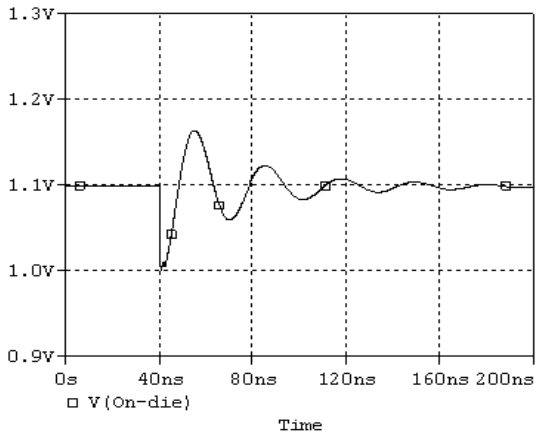

Figure 10. Simulated on-chip PDN voltage noise with one switching event.

Table 2. Comparison of simulation results and measured on-chip voltage noise.

	Voltage sag (mV)	Pk-pk (mV)	Resonant frequency
Measurement	105	172	33 MHz
Simulation	101	166	33 MHz

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VII. PDN Stimulus Definition

Previous sections have shown that on-chip PDN voltage noise could be 10 times higher than PCB PDN noise. To ensure the PDN robustness, it is vitally important to measure or simulate on-chip voltage under types of current stimulus created by system use. In this section, fundamental stimuli are developed to systematically characterize the on-chip PDN properties and voltage noise. Three fundamental PDN stimuli are impulse, AC steady state stimulus, and transient burst pattern.

A. Impulse stimulus

Impulse stimulus creates an impulse current drawn by triggering the circuitry to switch only once. Impulse stimulus is used to characterize test the impulse response of the system PDN. Figure8 shows a scope shot of on-chip voltage noise waveform with an impulse stimulus. All major system PDN properties can be extracted from the system PDN impulse response. First, the on-chip voltage sag and the over-shoot can be readily observed as discussed in a previous section. Second, the system PDN resonant frequency can be calculated as 33MHz based on the time interval between the first and second resonant peaks. Third, the Q-factor of the system PDN

can be roughly estimated as number of PDN resonant peaks. The fewer PDN resonant cycles, the lower the Q-factor, which is about 3 in this case.

B. AC steady state

AC steady state is defined as the condition where the circuit has been repetitively switching over many clock cycles, and the PDN current/voltage reach a steady state. Figure 11 shows the on-chip voltage waveform under AC steady state at different clock frequencies. The figure shows that the on-chip voltage noise reaches the maximum when the clock frequency equals the PDN resonant frequency since the circuit switching current is stimulating the PDN resonance. In this case, the PDN resonant frequency is 33 MHz. Beyond 33 MHz, on-chip voltage noise amplitude exponentially decreases with frequency, which matches the chip self impedance profile as shown in Figure 4. For this series of waveforms, the current drawn from the bench supply was proportional to the clock frequency.

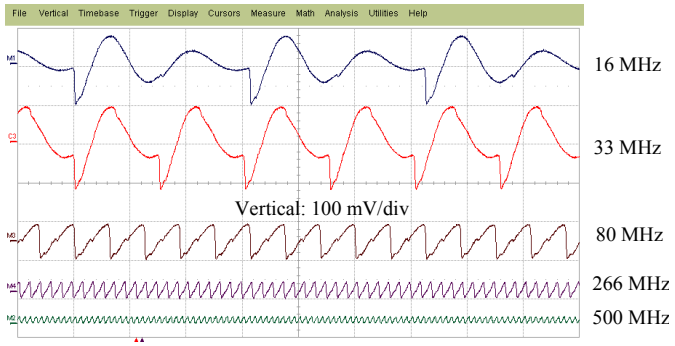

Figure 11. Measured on-chip voltage noise with different clock frequencies under AC steady state stimulus. Dynamic current is proportional to frequency.

C. Burst pattern

Typically logic toggles according to input data vectors. To characterize the interaction of the circuit switching current to the system PDN, a burst pattern is defined as a burst of circuit toggling activity after an idle state. Figure 12 shows one example of on-chip PDN noise under a burst circuit switching stimulus. The burst activity of all TFFs is defined by the clock signal, which is the third curve in the figure. For the first 10ns, the clock signal remains low so there is no switching. After the first 10 ns of idle state, a 266 MHz clock signal is fed into the TFFs, which causes the TFFs to toggle and draw current from the PDN. The second curve in the figure shows the corresponding on-chip voltage waveform. The on-chip voltage continues to sag for the first two TFF switching events because on-chip capacitance is the only available source of charge in that time frame. The maximum voltage sag is 137mV, which is 12.5% out of 1.1V nominal voltage. At the third TFF toggle, on-chip voltage starts to recover as the package and PCB starts to provide sufficient current to the chip, and on-chip charge starts to replenish. When the circuit stops drawing current at the end of burst stimulus pattern, this abrupt current change will cause a strong inductive overshoot as shown in Figure 12. The burst stimulus can be used to characterize the effectiveness of on-chip capacitance and the system PDN response time.

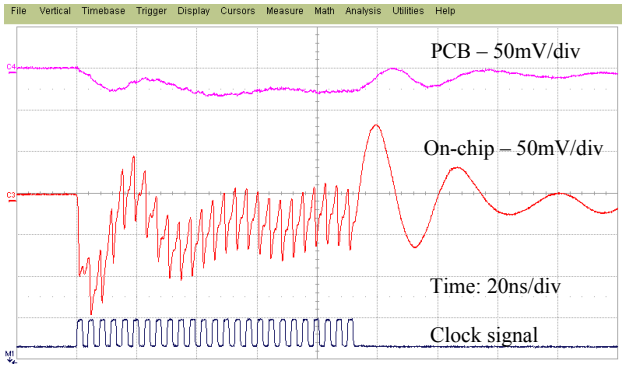

Figure 12. Measured on-chip voltage noise waveform with a burst pattern stimulus.

To characterize the system PDN robustness, a worst case PDN stimulus is developed. As illustrated by the third curve in Figure 13, a periodic burst pattern is defined as a burst of circuit switching following with the same number of idle states. When a periodic burst pattern repeats at the PDN resonant frequency, it will maximally stimulate and reinforce the PDN resonance due to its parallel inductive and capacitive resonant circuit nature and this will cause the strongest on-chip voltage swing. A periodic burst pattern at PDN resonant frequency is the worst case of PDN stimulus. In this case, with a 533 MHz of burst clock, the peak-peak on-chip voltage swing is 577mV, which is +/-26% over 1.1V nominal voltage. The on-chip voltage noise under this worst case PDN stimulus is dependent on the system PDN Q-factor and clock frequency. Lower PDN Q-factor and lower clock frequency will result in a lower voltage noise. Note that this measurement is for illustration purpose. In real designs, it is unlikely to have all logic synchronously toggling in a perfect periodic burst pattern at the PDN resonant frequency.

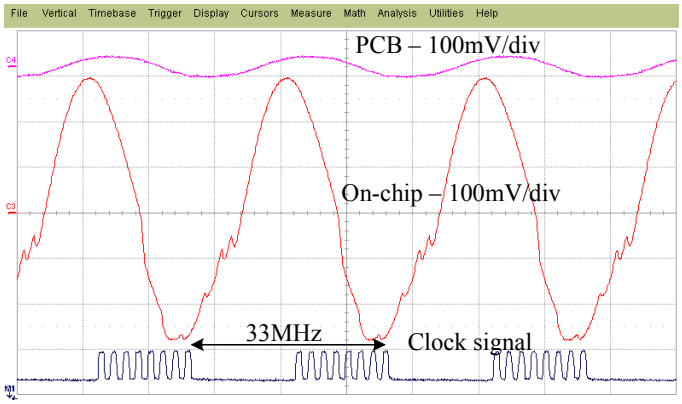

Figure 13. Measured on-chip voltage noise waveform with periodic burst pattern stimulus.

Figure 14 shows simulation results of the currents for the chip load, on-die capacitance (ODC) and the package under a periodic burst pattern at PDN resonant frequency, 33MHz. The simulation condition is the same as the measurement setup. Under this worst PDN stimulus, the package current is

resonating from +30A to -18A. The large negative current is the resonating current flowing out of the ODC, which results in a large voltage sag. The chip load current waveform shows a burst of eight current switching events following with 8 cycles of idleness. The current amplitude becomes smaller when the on-chip voltage decreases due to the voltage sag created by previous circuit switching events. For the ODC current, its envelop follows exactly the package current, but it shows fast spikes of opposite current as compared to chip load current. This simulation shows that the high frequency current of the switching circuit must be provided by ODC, and only the low frequency current is provided by the PCB PDN through the package.

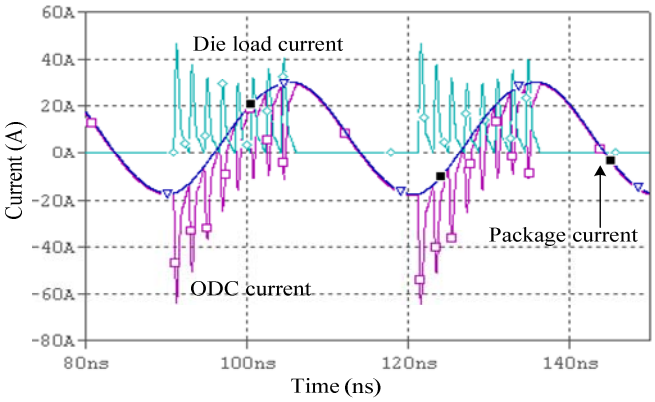

Figure 14. Simulated chip load current, package current and ODC current under periodic burst stimulus at PDN resonant frequency.

Table 3 summarizes and compares the voltage noise amplitude under different PDN stimuli. One important finding is that even with a well decoupled PCB PDN, the on-chip voltage noise is much higher than PCB PDN noise. Typical practice assumes that AC steady state type stimulus at the PDN resonant frequency is the worst case [5], but we have demonstrated that this is not the case.

Table 3. On-chip and PCB voltage noise amplitude under different PDN stimuli

		Impulse	AC Steady State	Burst	Periodic Burst @ 33MHz
Clock (MHz)			33	266	533
On-chip (mV)	pk-pk	172	232	228	577
	sag	105	139	146	281
PCB (mV)	pk-pk	11	18	36	48
	sag	7	9	28	24

VIII. PRBS Stimulus of PDN Resonance

With the fundamental PDN stimuli developed, generic noise injection method is proposed herein to mimic the variety of real use. To represent "randomness" of logic stimulus, a PRBS signal is used as the clock signal to drive the TFFs implemented in the test chip. The switching current is drawn by TFFs only at the rising edge of the clock. With a PRBS signal, the time intervals between two clock rising edges are variable, e.g., 2 T_o and 6 T_o as shown in Figure 15, the corresponding circuit switching frequency are *fclk*/2 and *fclk*/6 respectively. With a full sequence of PRBS signal, the circuit switching frequency spectrum will extend to all sub-rates of the fundamental clock frequency. The highest toggling frequency is $f_{clk}/2$, and lowest toggling frequency is $f_{clk}/(2^n-1)$, where (2^n-1) is the PRBS sequence length. Note that the Y-axis of the second figure in Figure 15 is the probability of specific PRBS switching frequencies, not the power or amplitude of PRBS harmonics. Due to the wide circuit toggling frequency spectrum, the proposed PRBS noise injection method can always stimulate the system PDN resonance no matter what is the PDN resonant frequency is, which will happen in real user activity. Figure 16 shows the on-chip voltage noise (the middle curve) with a PRBS 15 clock (the bottom curve). It clearly shows that when two sections of similar PRBS patterns drives the TFFs at a time interval of 30ns (33MHZ), a strong PDN resonance is stimulated. The peak-to-peak on-chip noise is 251mV in this case.

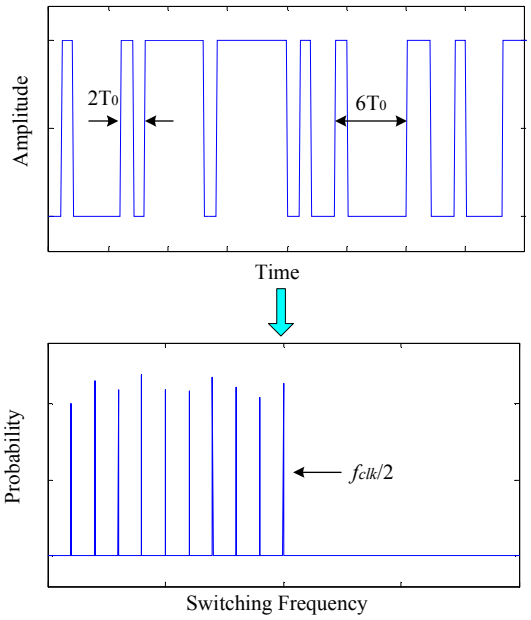

Figure 15. PRBS waveforms in the time domain and the corresponding circuit switching frequency spectrum when a PRBS signal is used as a clock signal

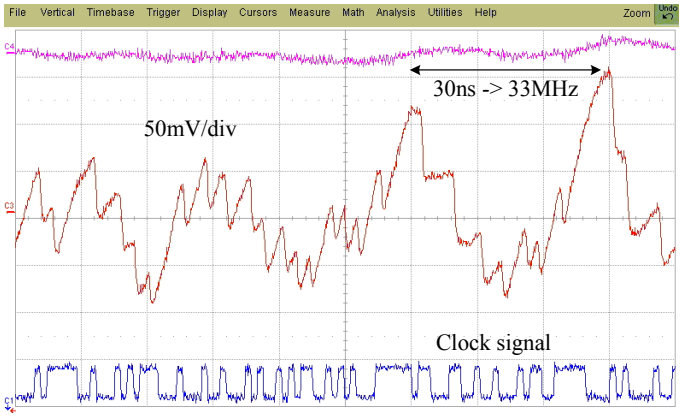

Figure 16. Measured on-chip voltage noise waveform when TFFs are dived with a PRBS clock signal.

IX. Timing and Jitter Implications

On-chip voltage fluctuation will reduce the circuit timing margin, and may cause functional failure due to timing violations. To understand the impact of on-chip voltage noise to logic timing, a clock network is used as a victim. The clock signal is connected to an external pin so the clock period jitter can be directly measured. Figure 17 shows a scope shot of the clock period jitter with respect to the on-chip voltage noise. The second curve in the figure shows the on-chip voltage noise waveform under an impulse stimulus. The bottom trace is the clock period for each clock cycle. As shown in the figure, the clock period is directly correlated to the on-chip voltage waveform. The first voltage sag causes a big jump of clock period due to slower CMOS operation under lower voltage. When the on-chip voltage resonates back to be higher than nominal voltage, the clock period becomes smaller than nominal 2ns period. The peak-to-peak clock period jitter is 169ps caused by 160mV of on-chip voltage fluctuation. The overall shape of the clock period waveforms inversely tracks to the on-chip voltage noise. This experiment clearly demonstrates the correlation between the on-chip voltage noise to the clock period jitter.

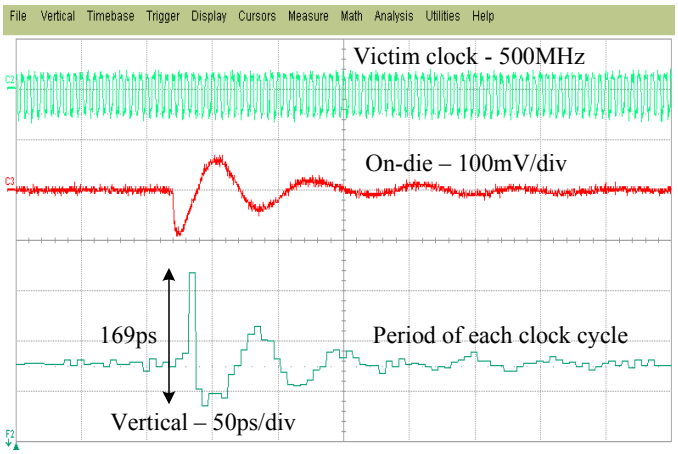

Figure 17. Measured clock period jitter under an impulse on-chip voltage noise.

X. Conclusion

Resonance in the power distribution network produces greater power supply voltage excursions than DC IR drop. The root cause is energy resonating back and forth between inductance (magnetic field) and capacitance (electric field) which are connected in parallel. The frequency and magnitude of the resonant peak impedance is a property of the system including the board and package inductance and the chip capacitance assuming reasonable PCB decoupling. The frequency domain peak is responsible for damped sinusoid ringing in the time domain. User activity and superposition enable waveforms to reinforce one another and often exceed the allowable voltage tolerance. The transient on-chip voltage noise is usually much higher than PCB PDN noise even with a well decoupled PCB. The system PDN properties and voltage noise can be systematically characterized with three fundamental current stimuli demonstrated in this paper. The worst case switching pattern is the periodic burst at the PDN resonant frequency. A PRBS pattern is used to represent a typical user activity.

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